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Low Power High Performance Multi-Gate Mosfet Structures

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Abstract

Increasing the need for MOSFETs in digital circuits, leads researcher to think beyond conventional MOS transistors. These fundamental limitations have given force to the continuous structural changes in MOS devices with remarkable progress. In the following sections, we have reviewed various MOSFET structures and designs based on different technologies to achieve low standby power dissipation, high ON-OFF current ratio and subthreshold performances under limits. Multi-gate MOSFET are promising candidates for future analog and digital design because of more control of gate over the channel and longer effective channel width. The new MOSFET structures are designed by using gate/channel engineering size shapes and materials to obtain optimum device performance in ON/OFF state of transistors. Several device design tool is available such as TCAD for any prefabrication design and analysis to ensure desired and reliable device performance. This paper mainly covers design of advanced MOSFET structures for DC and AC parameter analysis.

Keyword

High-K dielectric, DG MOSFET, FinFET, subthreshold performance etc.

1 Introduction

To address the scaling challenges of planar bulk CMOS technology, alternative MOSFET structures based on silicon-on-insulator (SOI) technology have been developed [1]. For SOI MOSFET, a buried oxide layer is formed on the bulk silicon substrate. There is a thin silicon film on the buried oxide layer where active MOS is located. Because of the buried oxide layer, the parasitic capacitances of SOI MOSFET devices are smaller than those of bulk MOSFET. Thus the delay of digital CMOS circuit due to junction capacitance can be reduced by SOI MOSFET. Also the power delay product of SOI CMOS circuit is much smaller as compared to bulk counterpart. Hence, we can say that SOI MOSFET has high speed and low power consumption.

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SOI MOSFET can be further divided into PD MOSFET and FD MOSFET [2] as shown in Figure 2.1(a) and (b). PD SOI was the basic SOI-based technology introduced for high-performance microprocessor applications. PD SOI MOSFETs offer a low power dissipation and better speed. For PD SOI MOSFET, the silicon film thickness is more than 50nm, which imposes the constraints on device V_{th} (threhslod voltage) and its sensitivity. Although the PD SOI device manufacturing is easier and compatible with traditional CMOS devices, it has some issues which are the floating body effect and the resulting parasitic bipolar effect. For, FD SOI, the SOI layer is much smaller than the depletion width of the device and its potential is tightly controlled by the gate. FD SOI also includes the elimination of floating body effect and better short channel effect. Therefore, FD SOI MOSFET is beneficial for low-power technologies.

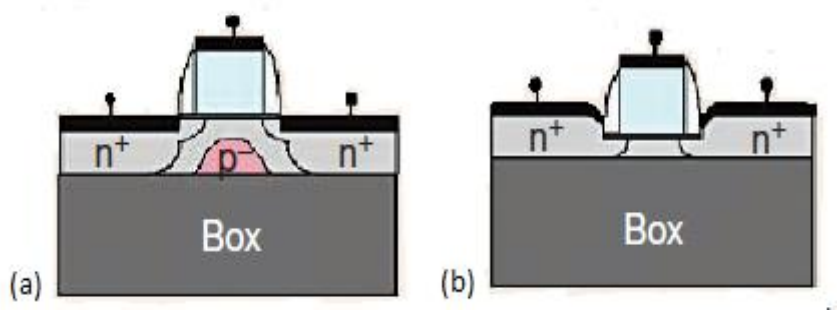

Figure 1(a) PD SOI MOSFET (b) FD SOI MOSFET with raised source/drain

The operating frequency of FD SOI transistor is higher than the conventional CMOS. Also, the FD SOI is more power-efficient than bulk CMOS as a result, devices run cooler and last longer.

2. Advanced MOSFET Structures

Multigate MOSFET [3] are promising candidates for future analog and digital design because of better subthreshold performance and longer effective channel width. The advanced MOSFET structures are double gate, triple gate or gate-all-around MOSFET showing the good value of ON/OFF current ratio and high switching speed.

DG SOI MOSFET

The DG MOSFET device structures have shown significant attention of the scientists and researchers in recent times [4-5] due to their natural suppression capability of the short-channel effects. The DG MOSFET has a sharp subthreshold slope, high drive current and high transconductance. An undoped

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or lightly doped symmetric DG MOSFET is generally preferred over a doped channel device because of its high carrier mobility and reduced doping-induced parameter variations. However, the feasibility of a negative threshold voltage in such devices with n+ polysilicon gates leads to an important technological challenge in the fabrication of the undoped symmetric DG MOSFETs. Thus a lot of interest has been shown by many researchers in recent times to study the subthreshold characteristics of asymmetric DG MOS device structure with a doped channel. According to this theory, short-channel effects could be optimized if the minimum gate length satisfies the condition of $L_g \geq 2\alpha\lambda$, where L_g is the gate length, α is a constant, and λ is the characteristic length. Here, λ is a function of device parameters such as the oxide thickness t_{ox}, dielectric constant of oxide ε_{si} and junction depth X_j or the body thickness t_{si} for ultrathin body MOSFETs. The standard device dimensions (t_{ox}, X_j, or t_{si}) can be fixed with given L_g.

The DG MOSFET can be designed as an asymmetric, asymmetric, tied and separated (Independent) device [6] as shown in Figure 2.4 (a), (b), (c) and (d). In, DG MOSFET, gates on both side of channel have similar work function with equal oxide thickness. In asymmetric DG MOSFET, gates have different work functions. Because metal-gate work function difference in asymmetric DG MOSFET at two interfaces, these devices have differences in threshold voltage and drain current. The asymmetric independent DG MOSFET requires a lower back gate voltage than the symmetric independent DG MOSFET to achieve a targeted threshold voltage. However, the asymmetric DG MOSFET is more sensitive to process fluctuation than the symmetric DG MOSFET.

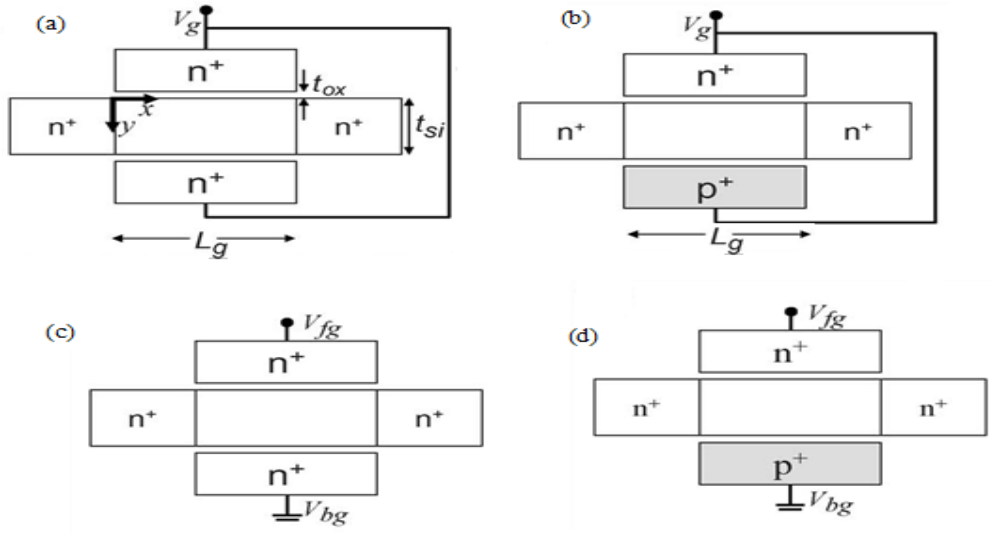

Figure 2.4 (a) Symmetric Double Gate (b) Asymmetric Double Gate (c) Symmetric Independent Double Gate (d) Asymmetric Independent Double Gate.

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TG SOI MOSFET

The Tri-Gate MOSFET (TG) have vertical thin channel with gate around all three of sides of channel. Since the gate control is increased, the scaling of Si film thickness in TG MOSFET is better implemented as compared to DG MOSFET. A transition from the DG to TG structures offers even higher drive current and increased immunity for SCEs compared to DG MOSFETs [6-7].

By reducing the channel dimensions (W, L and t_{Si}), ΔV_{th} is minimized, the subthreshold slope degradation becomes less severe, and the DIBL effect is most effectively reduced. Hence the possibility to obtain silicon TG MOSFETs of 30nm channel length and subthreshold slope approaching its ideal value of 60mV/decade at 300 K.

Bulk FinFET

Conventionally, FinFETs are fabricated on the SOI substrates [9]. However, SOI wafers have disadvantages with respect to their self-heating issues, defect density, cost and negative temperature bias effect etc. as compared to the bulk Si substrates. Bulk FinFET [10] structures with similar scalability and performances as SOI FinFET have also received significant interest from various groups. Bulk Si wafers, in addition to remove most of the disadvantages with SOI, are compatible with the existing planar CMOS process technologies, which is an important consideration.

The change of the subthreshold slope ($SS = S_0 + C * e^{\frac{T_b}{T_2}}$) is 4mV/decade per nanometer of body thickness variation. The DIBL ($DIBL = C_0 + C_1 * T_b + C_2 * T_b^2$) effect increases quadratically with the body thickness as shown in Figure 2.14 with DIBL variation rate around the 5-nm body thickness is 17 mV/nm.

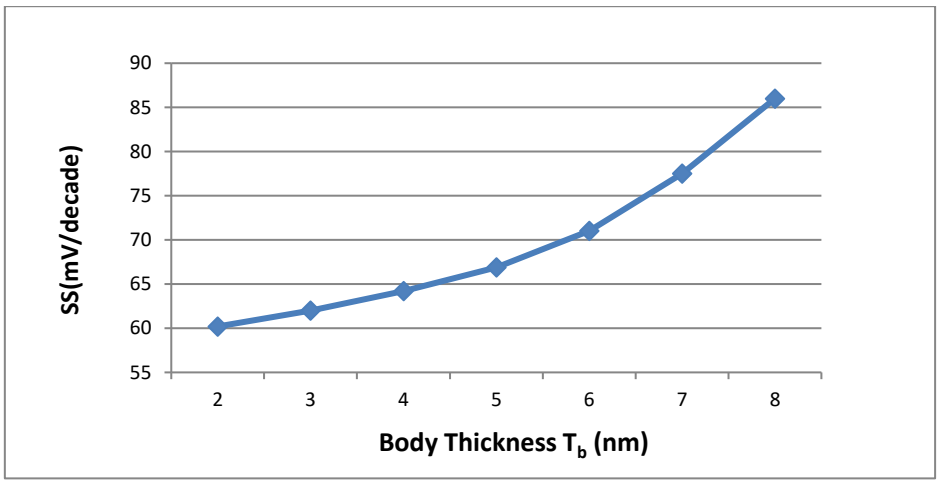

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Figure 2.13 Variation of subthreshold slope with body thickness for NMOS device.

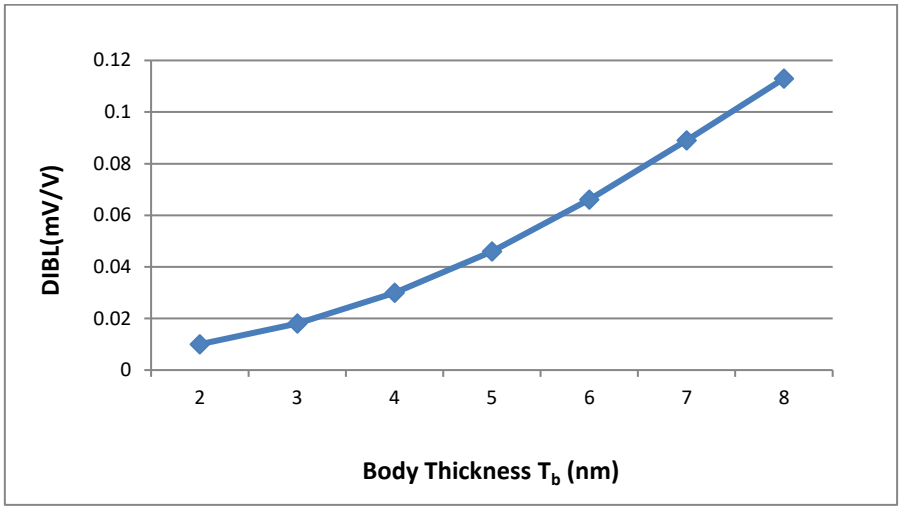

Figure 2.14 Variation of DIBL with body thickness of NMOS.

Further, the performance improvement of bulk FinFET comparable to SOI FinFET are modeled and investigated in various researches including body doping, Fin width and source drain junction depth variations [7-8].

Body Doping effect

Reported bulk FinFET [9] is similar to SOI FinFET except for the fact that bulk FinFETs use SiO_2 as isolation layer between the gate electrode bottom and the bulk Si surface to avoid gate electrode contacting the Si wafer as shown schematically in Figure 2.18. The bulk FinFET has introduced an undoped/moderately doped channel with heavier doping in the lower fin region which can be extended deeper into the bulk. It is better to all other doping profiles as it gives the lowest I_{off} and I_{on} multiplied by factor 2 with the optimized doping profile. Most of the bulk FinFET processes reported using a large isolation oxide that reduces the parasitic and use a heavy Fin doping to control the OFF-state leakage, which causes considerable mobility degradation. The term “upper Fin” is used to represent the Fin region which is mainly controlled by the gate and “lower Fin” to represent the Fin region which is covered by the T_{ins}.

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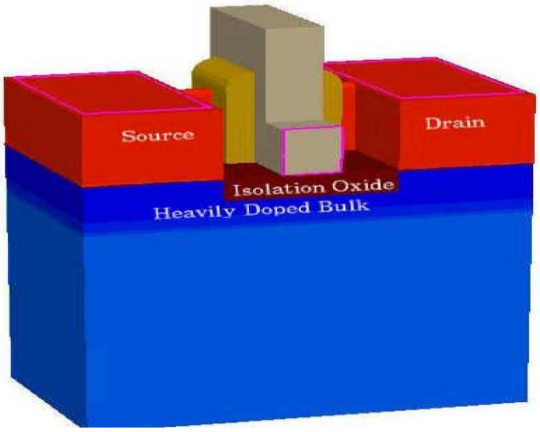

Figure 2.18 3-D view of bulk FinFET showing the patterned 3-D gate and bulk doping layer

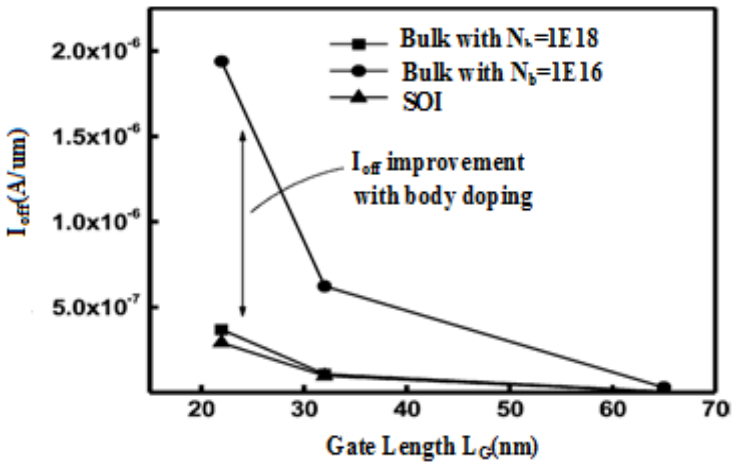

Figure 2.19 Variation of I_{off} with gate length for Bulk and SOI FinFET

Comparison of OFF-state leakage of SOI and bulk FinFETs, for various technology nodes ranging from 65nm to 22nm node is shown in Figure 2.19. It shows that with optimum body doping, OFF current of Bulk FinFET can be brought closer to that of SOI FinFETs. Figure 2.20 shows the variation of I_{off} with height of isolation oxide with and without doping. It can be seen that I_{off} is relatively insensitive to variation of height of isolation oxide in case of body doped bulk FinFETs. Bulk FinFET [9] with source/drain to body junctions depth shallower than bottom of gate has equal or superior subthreshold performance than SOI FinFET. By reducing S/D junction depth, Fin width scaling for reduction of short channel effects (SCEs) can be relaxed. The goal of such comparison is

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to find the bulk FinFET structure for a 45nm technology node with comparable or better characteristics than the SOI counterpart.

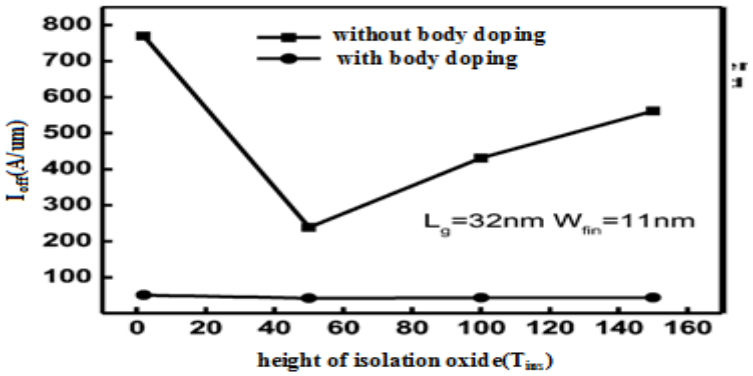

Figure 2.20 Variation of I_{off} with a height of isolation oxide with and without body doping

SOI FinFET

The FinFET is a self-aligned double-gate MOSFET structure with thin vertical channel region[10]. Self-alignment is important for reducing parasitic gate capacitances, series resistance and for control of the channel length. FinFETs are being considered as preferred devices for the sub-22-nm-node CMOS technologies. The vertical channel provides a wider device-width per unit wafer area, enabling FinFETs with more transistors packed in same silicon area. Bottom spacer FinFET [11-12] structure for logic applications is suitable for system-on-chip requirements with improved SCEs, self-heating and power delay. Figure 2.8 shows Bottom spacer Fin shaped field-effect-transistor (FinFET). The width quantization performance is compared with standard silicon-on-insulator FinFETs. Figure 2.9 shows that the proposed device shows a 20% higher inverter delay for the identical V_{th} case, while the other important advantages such as the short-channel performance and the power dissipation improve significantly.

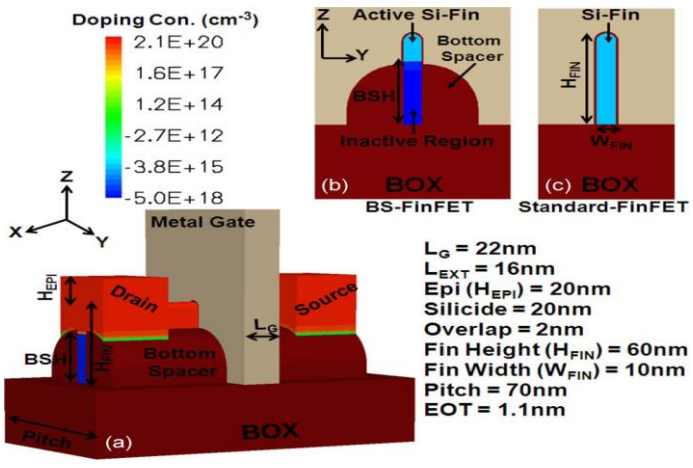

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Figure 2.8 (a) BS FinFET. (b) and (c) shows the difference between the Fin region of the proposed structure and the standard FinFET device.

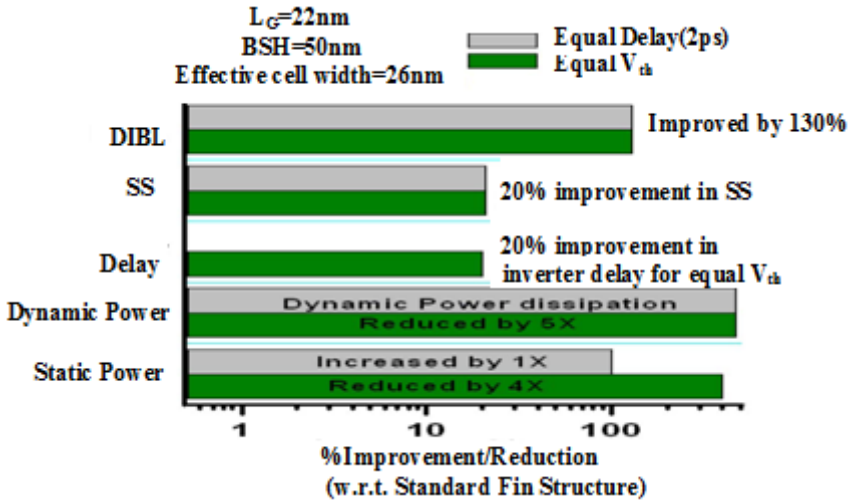

Figure 2.9 SCE and logic performance comparison of the proposed device and standard FinFET with H_{BS} = 50 nm for different cases (i.e., equal V_{th} and equal delay).

GAA MOSFET

For improvement in subthreshold slope (SS) and drain-induced barrier lowing (DIBL) of DG MOSFETs, the ratio of the Fin width to the gate length can be considered as an important design parameter. The critical dimension in devices is determined by the Fin width and not by the gate length, and therefore it appears as a barrier to aggressive scaling-down.

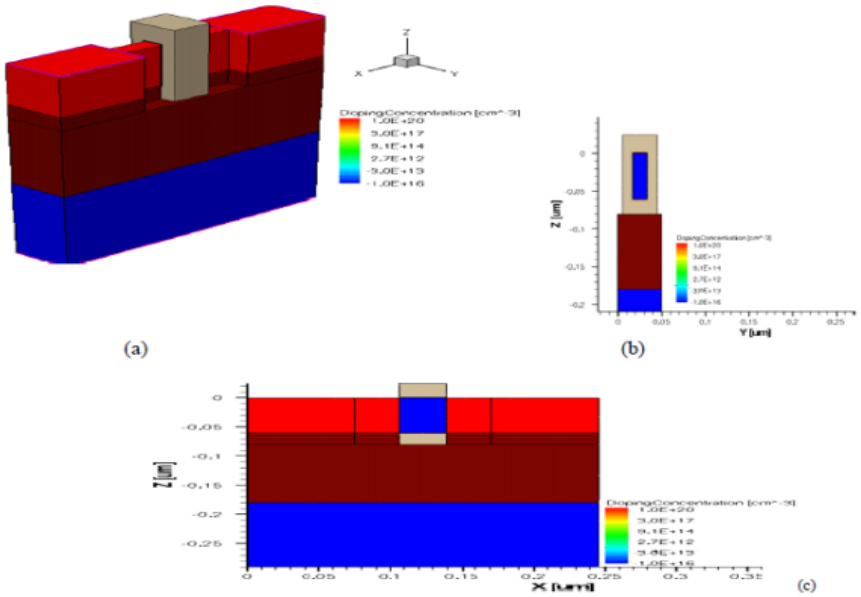

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Figure (a) GAA MOSFET (b) Y-cut GAA MOSFET (c) X-cut GAA MOSFET

The gate-all-around (GAA) MOSFETs in which the gate oxide and the gate electrodes wrap around the channel region show excellent transconductance and short channel behaviour because of the presence of four inversion channels and the occurrence of strong volume inversion [13].

3. Use of high –K dielectric materials

As devices are scaled down below a 30 nm gate length, the introduction of high-K gate dielectrics to replace SiO_2 becomes imminent to reduce the problems associated with gate tunneling [14]. A high-K material is an insulator with higher value of dielectric constant than silicon Dioxide (ε =3.9). High-K gate dielectrics, such as Al_2O_3, HfO_2,TiO_2 Si_3O_4, ZrO_2,[15] etc., have recently been adopted in the design of metal-oxide-semiconductor FET as an attractive to the conventional SiO_2 native oxide gate dielectrics, to reduce current leakage and increase the gate capacitance. The dielectric permits to modulate the carrier concentration of an adjacent semiconductor in a field-effect transistor. Scaling down of the high-*K* dielectric thickness is revealed to be favourable for device performance with a view to suppression of SCE High-K dielectric material is also suitable as spacer. FinFET with Dual material and triple material spacer have shown better subthreshold performance by inproving fringing electric field. Figure 11 shows a FinFET with dual material high-K delectric spacersFinFET with triple material high-k spacer give better performance when high-k dielectric material was kept adjacent to gate in comparison to single material spacer FinFET [16].

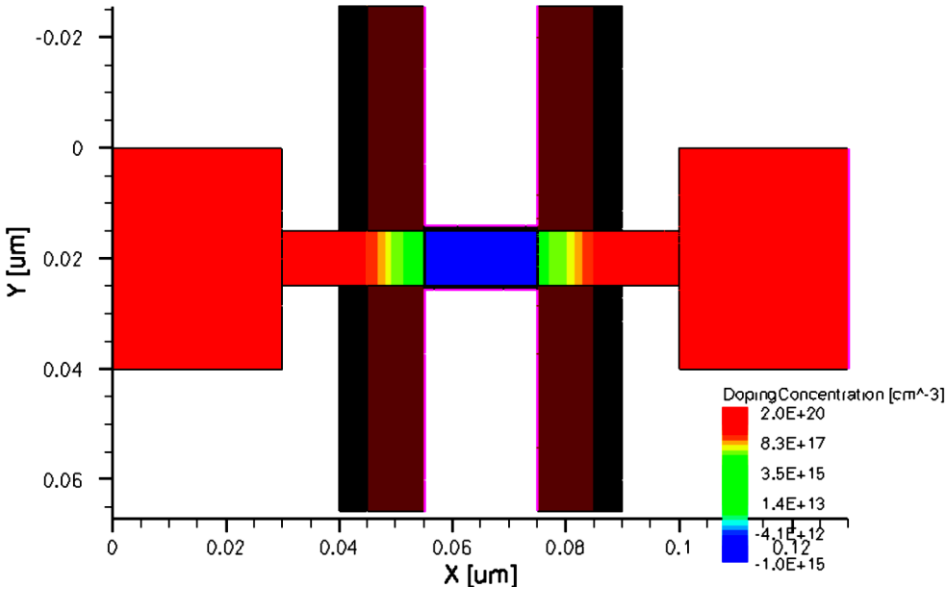

Figure 11 FinFET with high-K dual-material spacer

4. Junction-less FinFET

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Multigate MOSFET with junction-less transistors is used to achieve good On-state current because of absence of deletion regions. It acts like normally on transistor suitable to achieve good Ion/Ioff ratio with subthreshold performance under desired range [17-18].

5. Conclusion

An increasing number of gate increases the control over the channel and leads in the improvement of short channel effects of MOS Devices. In multi-gate structures, self-aligned FinFET has gained attention with lesser fabrication complexity as compared to conventional planner double gate and triple gate structures. Usually FinFETs are fabricated on SOI wafer because of its excellent short channel characteristics. But some disadvantages of SOI wafer over bulk FinFET like floating body effect, high wafer cost, heat transfer problem, negative temperature bias effect, have increased the importance of bulk FinFET structures. Further, introduction of high-K dielectric material has improved the performance parameters of MOS Devices and supported the scaling trends of these devices. The high-K dielectric material is suitable as oxide under gate or as spacer material to both sides of gate.

References

[1] E. J. Nowak, I. Aller, T. Ludwig, K. Kim, R. V. Joshi, C.-T. Chung, K. Bernstein, and R. Puri, "Turning silicon on its edge," IEEE Circuits Devices Mag., vol. 20(1), pp. 20–31, 2004.

[2] J.P. Colinge, "Fully-depleted SOI CMOS for analog applications" IEEE Transactions on Electron Devices 45(5), pp.1010, 1998.

[3] J.P. Colinge "The New Generation of SOI MOSFETs" Romanian Journal of Information Science and Technology, vol.11(1), pp.3-15, 2008.

[4] Jean-Pierre Colinge, "Multiple-gate SOI MOSFETs" Solid-State Electronics, vol.48, pp.897–905, 2004.

[5] L. Chang, S. Tang, T.-J. King, J. Bokor, and C. Hu, "Gate-length Scaling and Threshold Voltage Control of Double-gate MOSFETs" Int. Electron Devices Meeting Tech. Dig., pp. 719–722, 2000.

[6] Jin-Woo Han, Chung-Jin Kim, and Yang-Kyu Choi , "Universal Potential Model in Tied and Separated Double-Gate MOSFETs With Consideration of Symmetric and Asymmetric Structure" IEEE Transactions on Electron Devices, vol. 55(6), pp.1472-1479, 2008.

ISSN: 0971-1260
Vol-22-Issue-16-August-2019

[7]S L Tripathi, Ramanuj Mishra, R A Mishra, "Characteristic comparison of connected DG FINFET, TG FINFET and Independent Gate FINFET on 32 nm technology" IEEE ICPCES, pp.1-7, 2012.

[8] X.Huang, W.-C. Lee, D. H. L. Chang, J. Boker, T. J. King, V. Subramanian, and C. Hu, "Sub 50 nm P channel FinFETs," IEEE Trans. Electron. Devices, vol. 48(5), pp. 880–886, 2001.

[9]C. R. Manoj, Meenakshi Nagpal, Dhanya Varghese, and V. Ramgopal Rao "Device Design and Optimization Considerations for Bulk FinFETs" IEEE Transactions on Electron Devices, vol. 55(2), pp.609-615, 2008.

[10]D. Hisamoto, W. C. Lee, J. Kedzierski, J. Bokor, and C. Hu, "FinFET-A self-aligned double-gate MOSFET scalable to 20 nm," IEEE Trans. Electron. Devices, vol. 47(12), pp. 2320–2325, 2000.

[11]Mayank Shrivastava, Maryam Shojaei ,Baghini,Dinesh Kumar Sharma and V. Ramgopal Rao "A Novel Bottom Spacer FinFET Structure for Improved Short-Channel, Power-Delay, and Thermal Performance" IEEE Transactions on Electron Devices, vol. 57(6), pp.1287-1294, 2010.

[12]S L Tripathi, Ramanuj Mishra,V Narendra, R A Mishra, "High performance Bulk FinFET with Bottom Spacer" IEEE CONECCT, pp.1-5, 2013.

[13]S L Tripathi, Ramanuj Mishra, R A Mishra, "High Fin Width MOSFET with GAA structure" international journal of **VLSICS**, vol 3, pp.111-121, 2012

[14] Jean-Pierre Locquet, Chiara Marchiori, Maryline Sousa, Jean Fompeyrine, "High-*K* dielectrics for the gate stack", J. Appl. Phys., vol.**100**, pp.051-610, 2006.

[15] M. H. Chowdhury, M. A. Mannan, S. A. Mahmood, "High-k Dielectrics for Submicron MOSFET" IJETSE International Journal of Emerging Technologies in Sciences and Engineering, vol.**2**, pp.1-12, 2010.

[16] S L Tripathi, R A Mishra, "Performance improvement of FinFET using spacer with high k dielectric" in **JED,** vol 17, pp.1682-3427, 2013.

[17] Govind singh Patel, Suman Lata Tripathi, Sandhya Awasthi "Performance Enhnaced Unsymmetrical FinFET and its Applications" IEEE EDKCON, pp.222-227, 2018

[18] Suman Lata Tripathi, Sanjeet Kumar Sinha, Priti Gupta "Design of Triple material Junction-less CG MOSFET" IEEE ICICS, pp. 42-45, 2018

