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Review on Performance Evaluation of Tfet Structures & Its Applications

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Abstract:

Low power devices and low cost storage space are in huge demand in today's scenario of technological race. The tunnel field effect transistor (TFET) transistor is based on the carrier generation using quantum mechanical process of band to band tunnelling. TFET has the capability to meet the requirements of a device which can perform on low supply voltage with reduced leakage currents and also low Sub-threshold Swing (SS). TFET has quite similar type of structure as MOSFET but as far the switching mechanism is concerned, they are far apart. The different possible structures of TFET are described and comparison is done on the basis of above mentioned design parameters.

Keywords: BTBT, MOSFET, TFET, Sub Threshold Swing (SS).

I. Introduction:

Everyone in today's world desire the high end performing devices with least power consumption and the size of the same should be as small as possible. CMOSFET is widely used due to its ultra-low power (ULP) applications and TFET has the capability to replace the same. Different switching mechanism made TFET a different type of transistor having similar structure to MOSFET. The characteristics of TFET which makes it high performer are:

- Very low sub-threshold slope below 60mv/decade
- Application in low power systems
- Reduced leakage currents
- ON current to OFF current ratio is quite high
- Reduced short channel effects [1]

Taking into consideration the above parameters, the MOSFET could be replaced by TFET for the low power, high speed in energy efficient integrated circuits. Surface Tunnel Transistor is the first tunnel transistor proposed in 1978 at the Brown University as shown in Figure 1. After that first p-i-n structure based TFET was invented which deals with speed, power, IOFF/ION, tuning range etc. After that feedback TFET, Raised Buried Oxide TFET, Junction less TFET, Double gate TFET (DG-TFET), Dual Material Gate TFET, Hetero Junction TFET. TFET operation is based upon band to band tunnelling and it possesses very low leakage current and steep sub threshold slope. Sub threshold swing in case of MOSFET 1n(10)(KT/Q) and at room temperature (300k) ,SS value is around 60mv/dec. To reduce ss value 60mv/dec at room temperature can be easily overcome using a TFET device as shown in Figure 2. It also possess better ION/IOFF ratio as compared to MOSFET because of its low off current that TFET device is to be used in SRAMs for ultra low power applications. The 50% on chip area of the processor is occupied by the cache memory. To reduce leakage current in cache memory is serious one and it will be reduced immediately low off state current possessing of Tunnel FET device can be used.

II. TFET Structure and Operation

The basic TFET structure differs from a MOSFET structure in selecting different source and drain regions. Source is doped with p-type and drain is doped with n-type. The TFET device structure consisting a P-I-N (p-type, Intrinsic,

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n-type) junction with the intrinsic area is covered with oxide layer works on tunnelling between source and drain where the tunnelling potential is controlled by a gate above the oxide layer [2]. To understand the concept of tunnelling operation of tunnel diode is being discussed here.

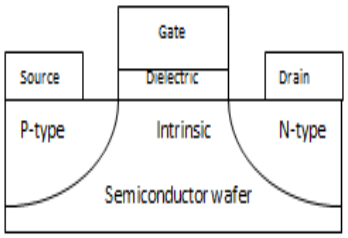

Figure 1. Basic TFET Structure

Tunnel diode is heavily doped in which depletion width is narrow. The electrons having higher energy will jump from n type to p type material for flow of current and those electrons which have lower energy may penetrate to potential barrier and called tunnelling of electrons. Even though they have lower energy they can tunnel through barrier and they can participate in flow of current.

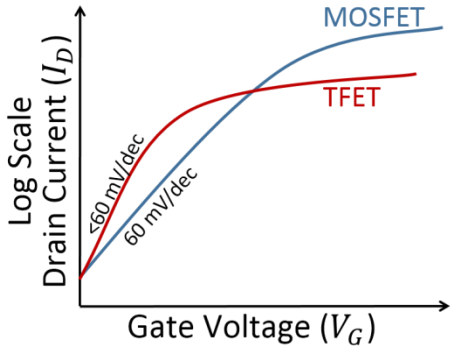

Figure 2. TFET Transfer Characteristics

If the voltage applied across the terminals of the tunnel-diode is less than the depletion layer built-in voltage, there will be no flow of forward current across the junction. However, a small tunnel current can exist due to the tunnelling of conduction-band electrons of n-doped region to the empty states of p-doped region valence-band. Thus, the flow of forward bias current in the form of tunnelling current starts by applying very little voltage. On the increment of the bias voltage across the tunnel diode, a large number of carriers are generated i.e. electrons in n-region and holes in p-region. The overlapping is enhanced between the conduction band and valence band with the increment in voltage. In other words, the energy levels of the conduction-band of n-doped region and valance band of p-doped region becomes almost equal which results in huge flow of tunnel current. With the further increment in the applied voltage, misalignment occurred slightly between the n-region conduction band and the p-region valence band takes place. Due to this the tunnelling current decreases but not stops flowing as the overlapping between the conduction-band of n-doped region and the valence-band of p-doped region still exists. Further increment of the applied voltage causes the tunnelling current reduced to zero. This stage indicates no overlapping exists between the conduction-band and valence-band and the operation of the tunnel-diode becomes similar to the regular pn junction diode. When the voltage applied reaches higher value than the depletion layer built-in potential of the tunnel diode,

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the negative forward current flow starts across the junction of tunnel-diode. The selective part of characteristic curve which indicates the decrement in the current with the increment in voltage is called the negative-resistance region of the tunnel-diode.

In order to increase a one decade in the tunnelling current, the amount of change in applied gate voltage is defined as the sub threshold swing of that device

$$S = \frac{dV_g}{d(\log I_d)} = \ln(10)\,\frac{mk_BT}{q} \qquad \text{eq.1}$$

III. Classification of Available TFET Structures.

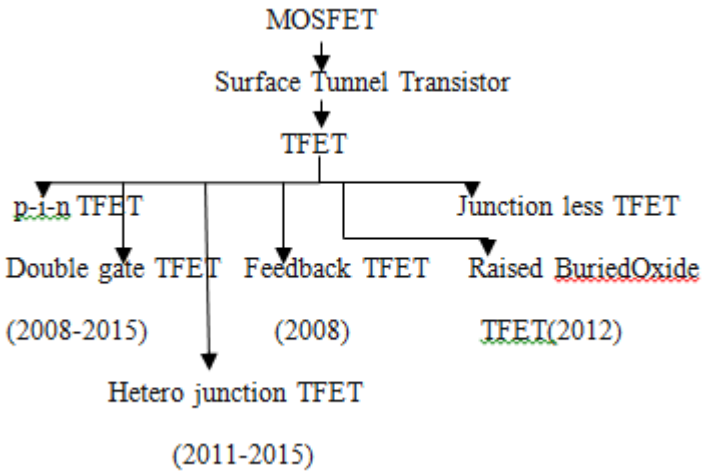

Figure 3. Classifications of available TFET structures

Evolution of Tunnel Field Effect Transistor

a). Surface Tunnel Transistor

The first transistor based on tunnelling was surface tunnel transistor consisting the p-i-n type structure with gate covering the area above intrinsic region but isolated through insulator as shown in Figure 4. The fabrication materials of source and drain are kept different to study the newly constructed device. The transfer characteristics of Surface Tunnel Transistor exhibit the action of transistor without saturation which is similar to the operation of vacuum triode. [3,4]

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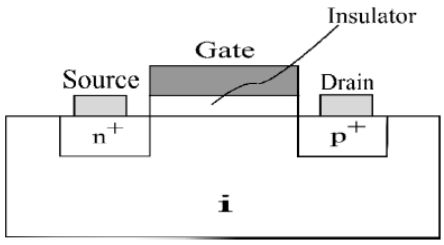

Figure 4. Structure of surface tunnel transistor

b). P-I-N structured TFET

It is different from the surface tunnel transistor in terms of buried oxide thin layer grown on the silicon substrate. First the silicon dioxide layer is grown on intrinsic layer and then source and drain region development followed by gate region. Source region and drain region are developed by required doping of n-type and p-type materials in silicon layer as shown in Figure 5. To block the leakage current between source and drain in SOI TFET, the whole intrinsic region of silicon is depleted and buried oxide layer blocks the possibilities of any leakage path. It enhances the gate controllability over the channel due to small depletion region of drain-body and source-body. This results in smaller capacitance between source/drain and substrate [5,6].

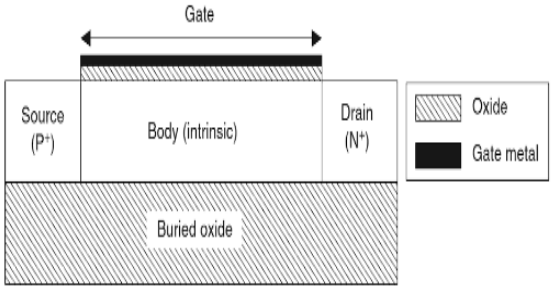

Figure 5. Structure of P-I-N structured TFET

c). Double gate TFET

Its structure includes two gates with two oxide layers fabricated at the top as well as at the bottom as shown in Figure 6. The electrostatic control of gate is improved over the channel as the termination of field lines occurs by the opposite gate rather than the channel. ON current is highly increased due to the creation of double channels for carrying the current. As the doping concentration of source cannot be increased arbitrary because the Fermi level will be raised into conduction band with the increase in doping concentration. The structure reduces filtering effect available on Fermi level within TFET and the sub threshold swing is degraded [7,8].

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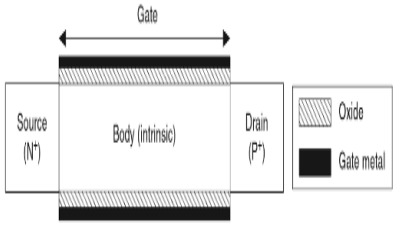

Figure 6. Structure of double-gate TFET

d). Hetero-junction TFET

In Hetero-junction TFET, different materials are used to fabricate the source and drain regions. Compared to homo-junction/normal TFET the higher tunnelling current can be achieved. The structure of a Hetero junction TFET device consisting of a P-I-N junction and the gate above the intrinsic region controls the electrostatic potential across the same. Hetero-junction TFET is normally utilised under the reverse bias condition. For carrier injection thermal injection mechanism is used as a source in MOSFET but in TFET, BTBT mechanism is utilized as a source for the same.

e). Doping less PNPN TFET

The PNPN Tunnel structure has a tunneling junction formed in between the p+ source and fully depleted thin n layer, in the gate as shown in Figure 7. It helps in reduction of tunneling width. Addition of thin n pocket region improves the tunneling rate, improves sub threshold and with the same instant of time gives maximum ION with respect to conventional design of TFET.

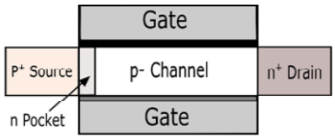

Figure 7. PNPN Tunnel Structure

Table 1. Device Performance parameters

Tunnel FET Device	Sub threshold swing (SS) in mV/dec	ON Current (ION) mA/um	Off current (IOFF) nA/um	Ioff to Ion ratio
Double gate Si TFET	116.3	0.00252	9.43x10^8	10^11

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Hetero junction Double gate TFET	95.64	0.0201	0.196	1.53x10^4
InAs based Double gate TFET	61.2	0.24	3.39	7.13x10^4

Table 2. Comparative analysis of PNPN TFET and Conventional TFET [10]

Lg(nm)		PNPN TFET		Conventional TFET		
	Ron (KΩ/μm)	SS(mV/dec)	Ion/ Ioff	Ron (KΩ/um)	SS(mV/dec)	Ion/ Ioff
30	42.6	53.1	10^8	64.1	93.2	10^5
35	46.1	55.3	4x10^7	61.2	90	10^5
40	48	62	6x10^7	60	91.2	0.1x10^6
45	48.5	65.6	4.2x10^7	58.6	91	0.2x10^6
50	50.2	68	10^7	57	90	0.4x10^6
55	53.3	72.2	0.6x10^7	53.8	72	0.7x10^6

BAND TO BAND TUNNELING

In TFET, tunneling of interest is band to band tunnelling. The occurrence of band to band tunnelling is due to the traveling of an electron from the valence-band of any semiconductor material to the conduction-band through the band gap without any assistance of available traps. The band gap plays the role of the potential barrier through which the particle tunnelled across. This phenomenon of tunnelling occurred between the valence-band and the conduction-band without absorbing of the photons or emission of the same is known as direct tunnelling. In the indirect tunnelling process the particle momentum gets changed by absorption or emission of a photon. There are almost negligible chances of the direct tunnelling process in the materials having indirect gap e.g. silicon as the probability of transmission decreases rapidly with the height of barrier.

OPTIMIZATION OF TUNNELING TFETs

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The optimization targets for T-FET are to achieve simultaneously the three important parameters. These are the maximum possible value of I_{ON}, the lowest average value of Swing obtained for different orders of drain current values, and the minimum possible values of I_{OFF}. For better performance than CMOS transistors, TFET should meet the following target parameters:

(i) I_{ON} should lie in the range of hundreds of mA,
(ii) Average value of Swing for 5 current decades should lie much below 60mv/decade.
(iii) I_{ON}/I_{OFF} ratio and Vdd should be less than 0.5V.

As Swing is directly proportional to the Vg, TFETs are automatically optimized and can be operated at low voltages. For obtaining high value of tunnelling current with steep slope, the probability of transmission through the tunnelling barrier source must be near to unit value for little change in Vg.

DOUBLE GATE TUNNELING EFFECT

Tunnel FETs with extra gate will be benefitted in an integrated type Double Gate Tunnel FET [11], if the I_{ON} current value becomes double at least. By this way, the ratio I_{ON}/I_{OFF} can be improved a lot because the ON current is doubled but the OFF current still lies in the range of pico-amperes even if it increases by the same factor.

APPLICATIONS:

TFETs or Tunnel FETs are similar to MOSFETs and applications of these two are similar like a digital switch, etc. The TFET belongs to the family of so called steep which are functioning at moderate frequencies slope devices that are presently being examined for ultra low power applications. Because of very low currents, they are perfectly suitable for low stand-by industrial metering, Telemetry, Asset and vehicle tracking, Wireless security systems etc.

- Analog/RF
- Product segments/applications which might benefit from STEEPER/TFET technology in future

Values of Various Parameters TFET

For the calculation of Drain current and probability all around FET, we use the following values of various parameters from some published papers.

Process parameters of Tunnel TFET

- Target application space
- Energy efficient nano electronic systems for high volume markets covering digital, analog/RF and mixed mode applications.

Transversemass (mnt)	0.19mo
Channel length Lc	10nm
Gateoxide Thickness (Tox)	0.77nm
Gatework function (o)	4.60
Gate voltage	0.7

CONCLUSION:

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In this paper, Tunnel FET provides the better performance in comparison with MOSFET and different structures of TFET are explained. It explained that the leakage power increases comes from scaling down dimensions without scaling down the supply voltage, and from trying to keep gate overdrive high by reducing threshold voltage IDS-VGS characteristics and thus increasing Ioff. Small swing device: TFET belongs to devices which have the small swing in sub threshold region. The sharp sub-threshold swing of TFETs results in a low Ioff and high Ion and hence, a higher ratio of ON and OFF current. Due to performance enhancement, TFET is more compatible to use for the power applications.

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