THINK INDIA Journal

ISSN:0971-1260
Vol-22-Issue-16-August-2019

Architecture of Flash ADC

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Abstract—Flash ADC are considered as fastest one due to its parallel architecture but it consumes lot of power due to large number of component and their complex arrangement. By systematic arrangement of input or output power consumption is considerable saved without much affecting the conversion speed. A conventional flash ADC consumes more power due to large number of comparator and more switching in the encoding circuitry. In this research paper 2 different architecture of flash ADC explored; 1st type of ADC focused to reduce number of comparator but size of multiplexer at the encoding part increases. 2^{nd} type of ADC does not required resistive ladder at the input it utilizes ^{2n}-1 number of TIQ comparator and simple arrangement of multiplexer in encoding circuitry. Cadence spectre based simulation at cmos 90nm technology verify that flash ADC with algorithm at input consumes more power 1.55mw while flash ADC with algorithm at consumes very less power 14uw.

Keywords—Flash ADC; Comparator; TIQ; Thermometer Code; high speed encoder; low power encoder

I. INTRODUCTION

Analog to digital converter (ADC) is an important module which converts analog signal into equivalent digital signal. There are a number of architectures of ADC are available (a) pipeline ADC(b) successive approximation ADC (iii) dual slope ADC (iv) sigma-delta ADC and (v) flash type ADC. Flash ADC is the fastest converter among all other types of ADC due to its parallel architecture. Two different type of flash ADC are in practice (i) Input of ADC are arranged to generate different reference voltage [1]. A voltage divider circuit requires; implemented using resistor ladder. In this case a single code converter required at the output. (ii) Output of ADC are arranged to generate output bits [2] [3]. In this case input voltage compared with TIQ comparator; multiplexer based encoder used to generate output bits. A TIQ based flash ADC does not required resistor ladder. Figure1 shows the basic architecture of flash adc; requires resistor ladder and thermometer binary code conversion. Resistor ladder is the major source of power consumption. In 1st type of ADC algorithm is applied at input which reduces the number of resistor and comparator; 2^{nd} type of architecture algorithm at output contains TIQ comparator and efficient code conversion process[4-7]. Speed of ADC is the summation of delay of comparator and delay of binary code conversion. Delay of comparator is the limiting factor to determine conversion speed of ADC. Since input signal applied to each comparator parallel so the conversion is very fast. Structure of paper is organized as follows section 2 describe the flash ADC architecture and their comparative analysis is reported section3.

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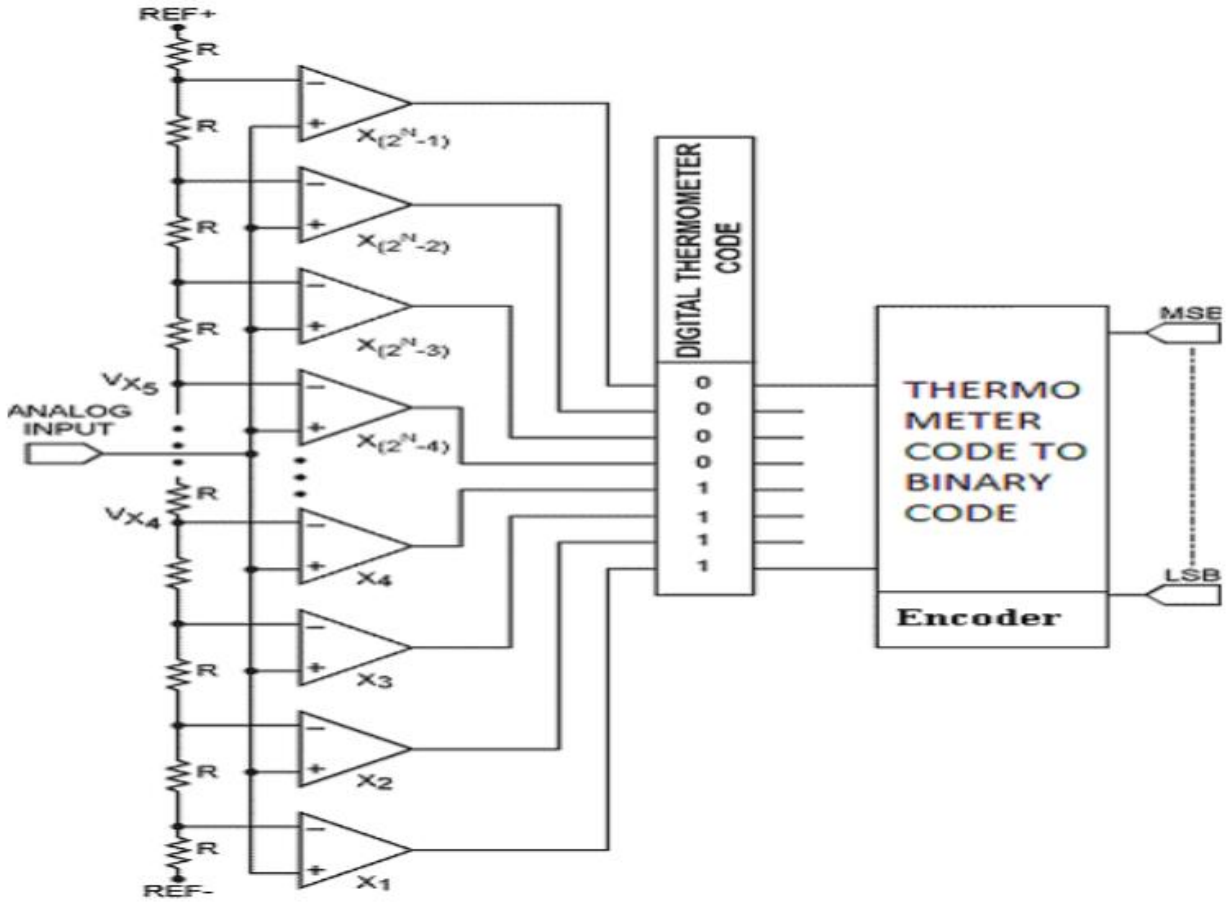

Fig. 1 Block Diagram of Flash ADC [1]

2. Architecture of flash ADC

A. Flash ADC architecture with algorithm at input

An n-bit flash ADC[8] consists of 2^n resistor ladder, 2^n-1 comparator and thermometer to binary converter. Resistor ladder network is a series connection of 2^n-1 resistor, used to generate reference voltage of each comparator it compares with input signal. When the input voltage crosses the reference voltage of comparator generate"1", otherwise the comparator output is "0". Comparator delivers the comparison result as thermometer code (string of 0 and 1).This thermometer code will encode thermometer code into a binary. Output of comparator is followed high bit by high speed encoding. Working of encoder is similar to 1 counting circuit, it counts number of one in the thermometer code and generate equivalent binary code. Table-1 represents the switching voltage of binary for sinusoidal input. In this work multiplexer based fast encoding has been implemented. Conversion algorithm is shown in fig2, Output of comparator and multiplexer works as select line of followed multiplexer. Input of ADC contains potential divider network (not shown in diagram) which divides input voltage into 16 different steps. Potential divider implemented using resistor ladder network and NMOS ladder network. Resistor ladder[9-14] is the major source of power consumption can be replaced using nmos acting as resistor.

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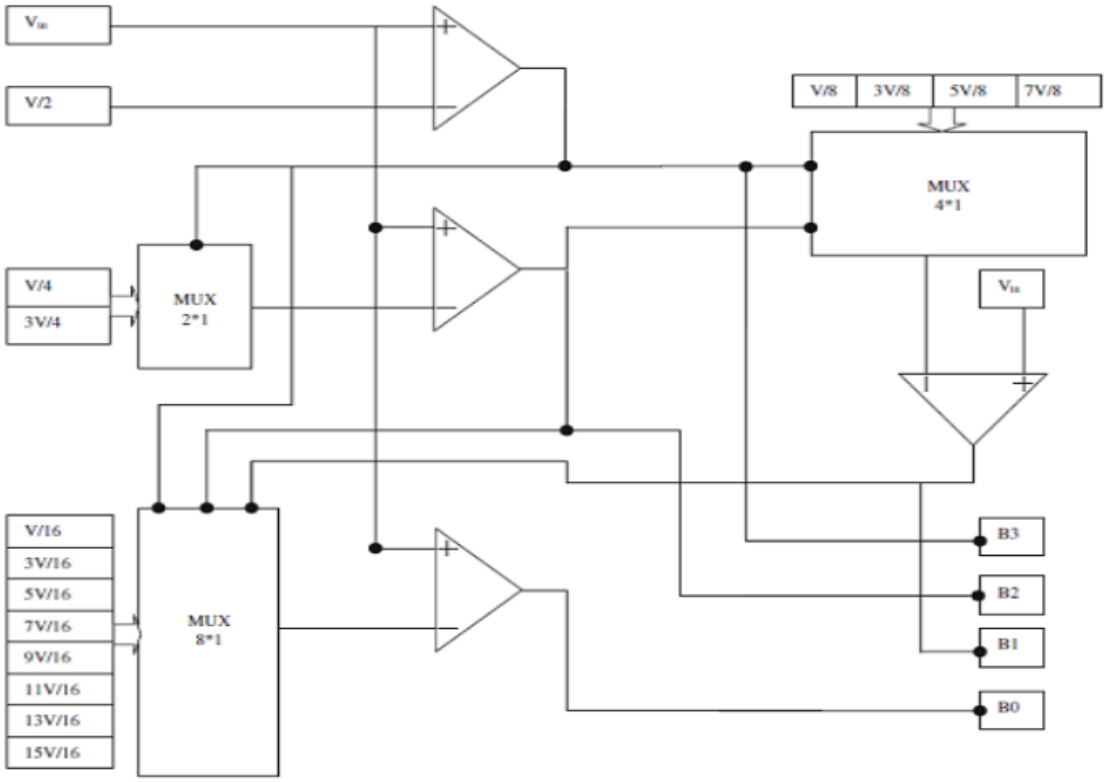
Figure3 shows the simulation result of flash ADC for sinusoidal and ramp input signal at supply



voltage 3V.

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Fig. 2 Flash ADC with algorithm at input [1]

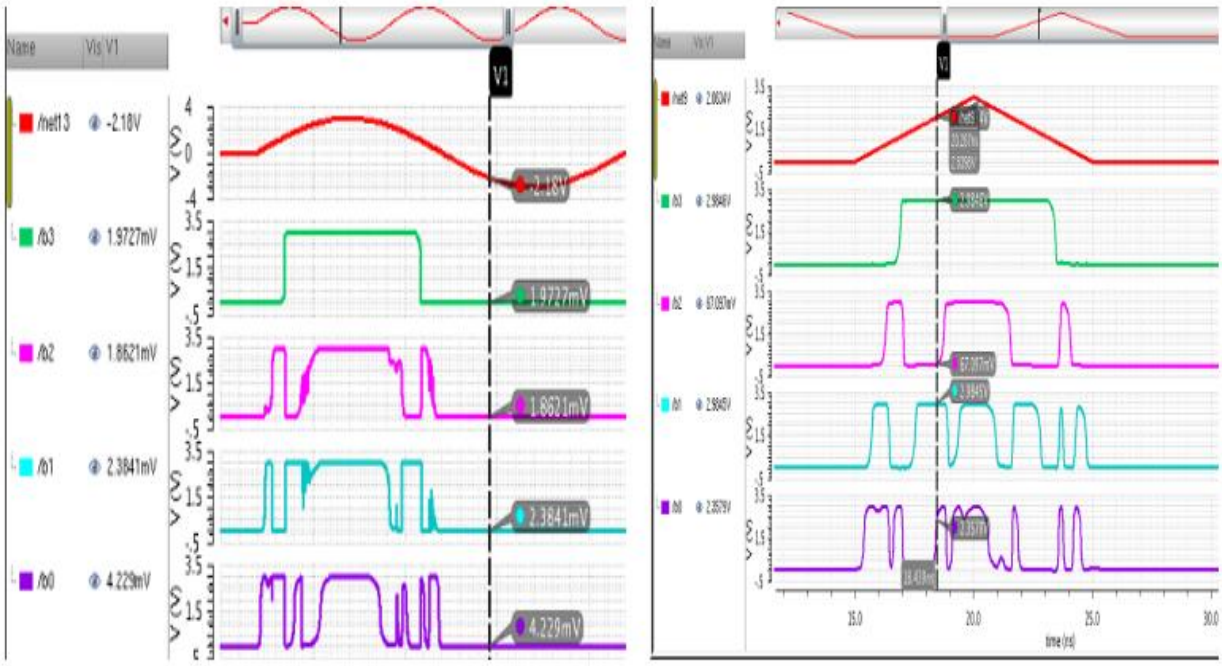

Fig. 3 Simulation of 1st type flash adc for sinusoidal and ramp input

Table1 Switching voltage of flash adc at supply voltage 3V

Binary Output	Switching Voltage(v)
0000	0
0001	0.3
0010	0.448
0011	0.627
0100	0.804
0101	0.961
0110	0.99
0111	1.0
1000	1.01
1001	1.33
1010	1.93
1011	2.1
1100	2.3
1101	2.47
1110	2.64
1111	2.81

ISSN:0971-1260
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B. Flash ADC architecture with algorithm at output

Another type of flash ADC architecture contains Threshold Inverting Quantization (TIQ) comparator and thermometer to binary code converter. TIQ comparator is a cascaded connection of 2 inverters. First inverter generates switching voltage internally and second inverter acts as gain booster. Figure4 represents schematic of TIQ comparator. For a given analog input, the comparators generate different dc levels and generate corresponding thermometer codes. These thermometer codes are converted to Binary by an encoder [15,16].Total conversion speed of ADC depends on comparator switching speed and encoder. It is required to have fast comparator speed which leads to high power consumption. The TIQ comparators compare the input voltage with in-buit reference voltages, which are determined by the transistor sizes of the inverters and generate input and delivers thermometer code. By changing the width of pmos while nmos width kept constant different threshold of inverter can be obtained. Function of inverter threshold voltage is similar to reference voltage of resistor ladder in conventional ADC. Each of TIQ comparator switches at specific reference voltage,. Switching voltage of each comparator has been determined by (1) for different value of Wp

$$V_{switching} = \frac{\sqrt{\frac{\mu_p W_p}{\mu_n W_n}}}{1+\sqrt{\frac{\mu_p W_p}{\mu_n W_n}}}(V_{DD} - |V_{tp}) + V_{in} \qquad (1)$$

Table 2 contains the obtained switching voltages of design, when width of PMOS is varied by maintaining transistors length and NMOS width constant. Same switching voltage can be obtained mathematically by equation (1) [17,18] for different PMOS width and DC analysis of TIQ comparator are almost accurate. Each comparator generated different thermometer code for each switching voltage for supply voltage 0.8V.Figure6 shows the dc analysis of TIQ comparator for variable width, crossing point of input and output represent switching voltage.

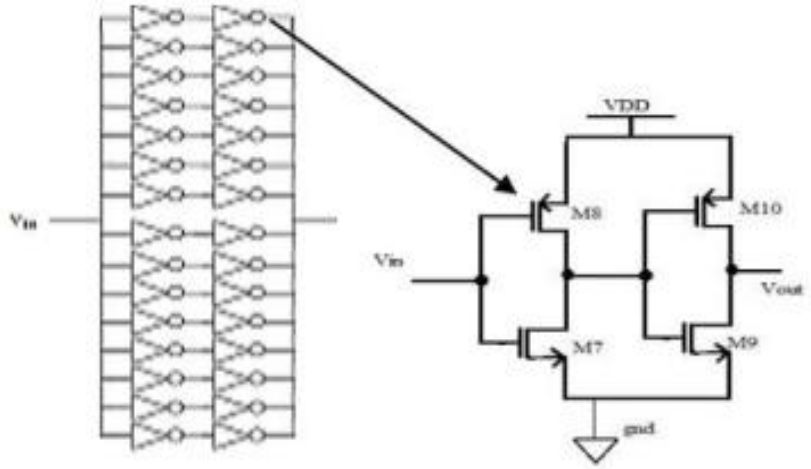

Fig. 4 TIQ Comparator [4, 8]

Table2 Switching Voltage of TIQ comparator for variable width at supply voltage 1V

Wn(µm)	Wp(µp)	Vs(v)
0.12	0.12	0.336

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0.12	0.215	0.358
0.12	0.285	0.371
0.12	0.385	0.384
0.12	0.685	0.41
0.12	0.92	0.421
0.12	1.225	0.43
0.12	1.64	0.442
0.12	2.195	0.455
0.12	2.935	0.467
0.12	3.925	0.473
0.12	7.015	0.496
0.12	12.545	0.513
0.12	22.435	0.53
0.12	30	0.542

Next stage of analog to digital converter is high speed encoding. Several method has been discussed in [7-9] for encoding style. Multiplexer based encoding style is the most efficient and consumes less power. The encoder designed with two 2x1 Multiplexers and two 4x1 Multiplexers and one 8x1 multiplexer shown in figure5. This encoding style is popular due to its low power consumption. The outputs of comparators are connected to the appropriate multiplexers so as to convert the Thermometer codes to respective Binary codes. Figure6 presents simulation result of TIQ based flash ADC for sinusoidal input signal amplitude 0.8V and frequency 800MHz.

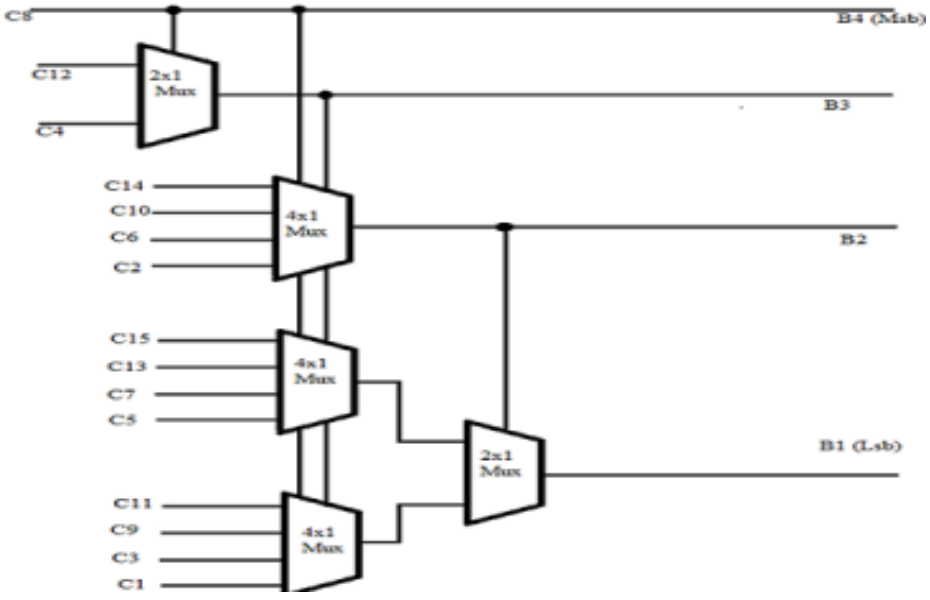

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Fig. 5 Encoding circuit

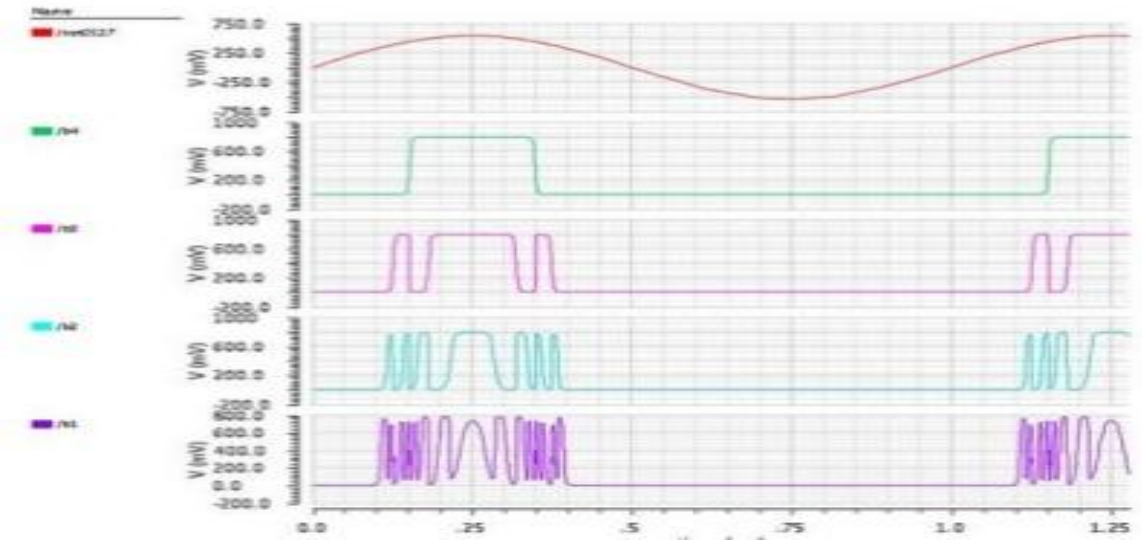

Fig. 6 Output of TIQ based flash ADC for sinusoidal input

III. CONCLUSION

In this research paper two different architecture of flash ADC has been implemented with and without resistor ladder. Table 3 represents comparison of both architecture of flash ADC. 1st type of ADC architecture is suitable of high speed conversion but requires more power while TIQ based ADC is suitable for low power flash ADC. 1st ADC architecture has efficient conversion process it uses only four comparators instead of 15, but it consumes more power 1.55mw. To reduce power resistor ladder designed using Presistor; power consumption reduced to 86uW while NMOS as resistors in resistor ladder power consumption reduced to 67uW. To further reduce power, eliminate power hungry resistors; using TIQ as comparators in flash ADC architecture has shown a very good impact on power consumption only 14uW and delay 215us.

Table3 Performance analysis of flash ADC architecture

Parameter	Type-1 Flash ADC	TIQ Comparator based flash ADC
Technology	CMOS 90nm	CMOS 90nm
Transistor Count	High	Low
Power	1.55mw	14µw
Delay	239ns	215ns
INL	i0.263 LSB	i0.59LSB
DNL	i0.45LSB	i0.2LSB
ENOB	i2.49bits	i2.7bits

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