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Design and Analysis of Power an Efficient Hybrid PLL For Communication System

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ABSTRACT: The proposed work presented parametric analysis of the PLL communication system**.** The wireless personal communication market has been growing explosively due to ever rising new applications and dropping prices. A low monetary value, small size, long-battery-life solution has been the ambition for decades. Many researches are being done for the development of such circuits using a cost effective technology in order to reach the goal. The applications of wireless communication devices include cellular mobiles, tuners, televisions, global positioning systems, wireless local area networks, cordless phones and transmitters that transmit either voice or data.

KEYWORDS: - VCO, FPGA, Loop Filter, Phase Detector, Xilinx.

I INTRODUCTION

PLL is an important device that is used to generate different frequency for various applications. Power is an important criterion in various communication systems. For many manufactures and product developers it is a good idea to reduce the use of power. Among collection of frequency synthesizers that are present the fractional N phase lock loop plays the predominant role in the industries of wireless communications. In general PLL frequency synthesizer contains phase detector, loop filter, Voltage Controlled Oscillator and frequency divider. It will be designed using Xilinx tool. We have various methods to implement frequency synthesizers. Among all those this fractional N- PLL frequency synthesizer is considered the more efficient and most widely used because of its low power consumption and high speed and its ability produce wide range of frequencies.

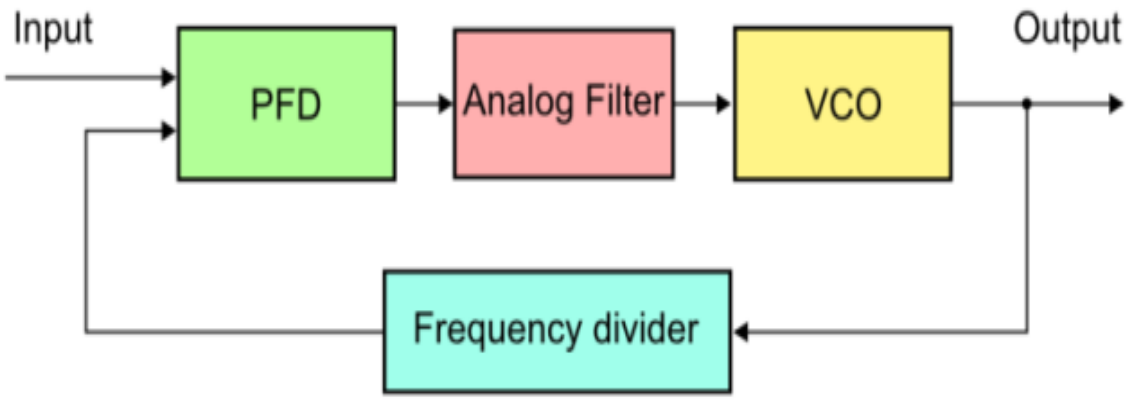

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Figure 1: PLL block diagram

Figure 1 shows block diagram of PLL. It consists of phased detector, low pass filer, VCO and divider.

II LITERATURE REVIEW

The various researchers give their view in the following review papers as follows:

Li Lin [1] has elaborated the different design techniques and described each step to implement a frequency synthesizer. The author also proposed the prototype of a synthesizer using PLL architecture and implemented using 0.35µm 2-poly 5-metal CMOS process. The author also says that among all the designing architectures of the frequency synthesizers the wide-band PLL is more gives the high performance.

K.Deepa, R.Shankar [2] have proposed the concept of the SCVCO which is Source coupled Voltage Control Oscillator they say that it even though it consumes more power and area it is more efficient than VCO which gives more phase noise. It provides the complete circuit of PLL synthesizer and it is designed using 180nm technology in CADENCE tool and analysis of the noise performance and frequency oscillation is given.

M. Houdebine and S. Dedieu discussed [3] the implementation of frequency synthesizer using 45nm in micro wind software. This deals with the detailed explanation of the each block of the circuit with their specifications and the parameters.

This Works focused[4] on Intel's 45nm CMOS Technology. It briefly explains the process of 45nm Design for Manufacturing and also discussed the detailed information of the high-k+metal gate transistors that have been begun for the first time into high-volume fabrication.

T. Ananthapadmanabha, A.D. Kulkarni , Radha. R and Pramitha Udupa [5] described the demand for the frequency divider and what their role is in the PLL circuit. They also elaborated the various design techniques of different frequency dividers and specifications to implement a frequency divider in cadence tool.

Wancheng Zhang and Nan-Jian Wu [6] described the important parameters that are to be considered for making a PLL frequency synthesizer. He described about the terms Reference Spurs, Phase Noise, Lock Time, Frequency Reference and the lock importance of lock time. He also explained why the PLL synthesizers are so famous and their advantaged over others. He said where they are being used and their purpose in the real time.

Sung Tae Moon [7], the author has given the details for implementing the each block of the circuit using CMOS technology and their specifications and also the analysis of testing wave forms .He also given the working and applications of the PLL.

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Tunduli W Michael [8] discussed the various applications of the PLL synthesizers in the real world and their purpose in detailed manner and also explained the different methods to obtain a PLL synthesizers of high performance with low phase noise, high frequency and low chip area.

R K Patil, V G Nasre [9] has described that to achieve stability we need to use a resistor in series with capacitor. He also explained how implement a power efficient frequency synthesizer with high performance. He used CSVCO current starved voltage control oscillator in implementation of PLL frequency synthesizer.

Young Gun Pu, An Soo Park, Joon-Sung Park and Kang-Yoon Lee [10]explained how the XOR can be used as phase detector and how to implement it by using micro-wind software and he also explained the working of loop filter as a charge pump using RC circuit and the design of PLL is explained briefly by implementing each block individually.

Fadhilah Binti Noor, Nabihah Ahmad and M. Hairol Jabbar1[11], claimed that implementing a low power consuming and high frequency PLL system is their main target. They have done it by using 130nm CMOS technology in cadence tool. They proved that by using MTCOMS in cadence we achieve low power consuming high frequency synthesizer. This paper helped us in understanding output wave forms and their parameters in lock condition.

P. Hanumolu, M. Brownlee, K. Mayaram, and U. Moon explained [12] his research work and implementation of 30 GHz PLL frequency synthesizer. He has described the terms that we should take care of while implementing a PLL frequency synthesizer such as Leakage current, Timing mismatch, charge pump mismatch, Tuning range and gain, power dissipation, oscillation voltage. He described the design process using different frequency dividers such as D-type flip flop dividers, Current mode latch dividers, and Injection locked frequency divider.

J. Nageswara Reddy, R..P. Singh [13], These writers has created a PLL by using 45nm technology in CADENCE software. They said that this PLL has given much less lock time. The lock time of the PLL depends on the Phase detector that we use in circuit and also on the parameters of the low pass filter and the charge pump. They said that the size of transistor must be considered among the major factors because of frequency depends on size of transistors.

Navid Azizi, Muhammad M. Khellah, Vivek K. De, and Farid N. Najm [14] designed the PLL frequency synthesizers that are used in ZIGBEE applications over a wide range of frequencies(2.4Hz). They said that the VCO is the major component of the PLL frequency synthesizer. They have implemented a CSVCO (Current Starved Voltage Controlled Oscillator) which has a wide range of tuning frequency. They have done this

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using 45nm CMOS technology on CADENCE software. They proved that this PLL synthesizer produce a faster lock in time and uses low power.

J. Tusch described [15] the design techniques of various phase detectors like D- flip flop phase detectors, XOR phase detectors, sample and hold phase detector, RS latch phase detector, bang-bang phase detector and also explained the difference between analog and digital phase detectors. They have mentioned the design issues such as phase lock time, the sensitivity of the phase detector and illustrated the ways to overcome those issues in a efficient manner.

D. Sahu [16] presented that in order to achieve a PLL synthesizer with no error in the phase and frequency of the signal that is being transmitted or received we need to maintain the jitter in a minimum amount. They described that the bandwidth of the signal and noise are inversely proportional to each other. That said how to achieve a low jitter by reducing the supply noise and the increasing the bandwidth of the signal. They have also explained the each block of PLL individually and explained the output wave forms that they have obtained.

S. Dosho and N. Yanagisawa [17] said that while designing a Voltage Controlled Oscillator the selection of inductor plays the major role. They explained the physical mechanism of the each components of the VCO. They have designed the LC oscillators in cadence and described the constraints one must follow in implementing the circuit.

III SIMULATION AND RESULTS

Figure 2 shows the RLT of the proposed technique. It is an internal diagram which presents the working of the PLL.

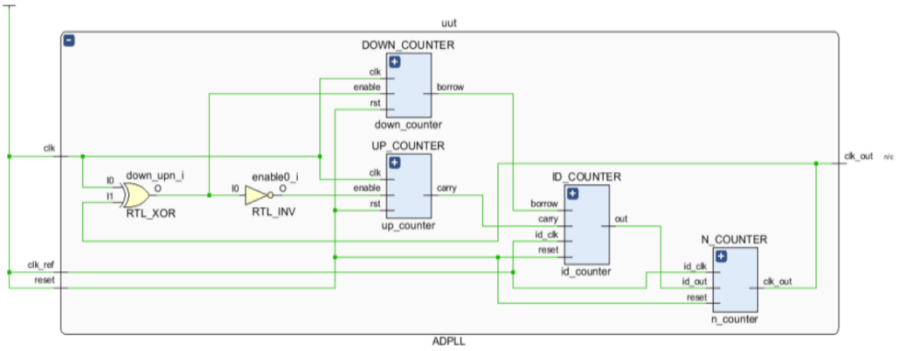

Figure 2: RTL of proposed architecture

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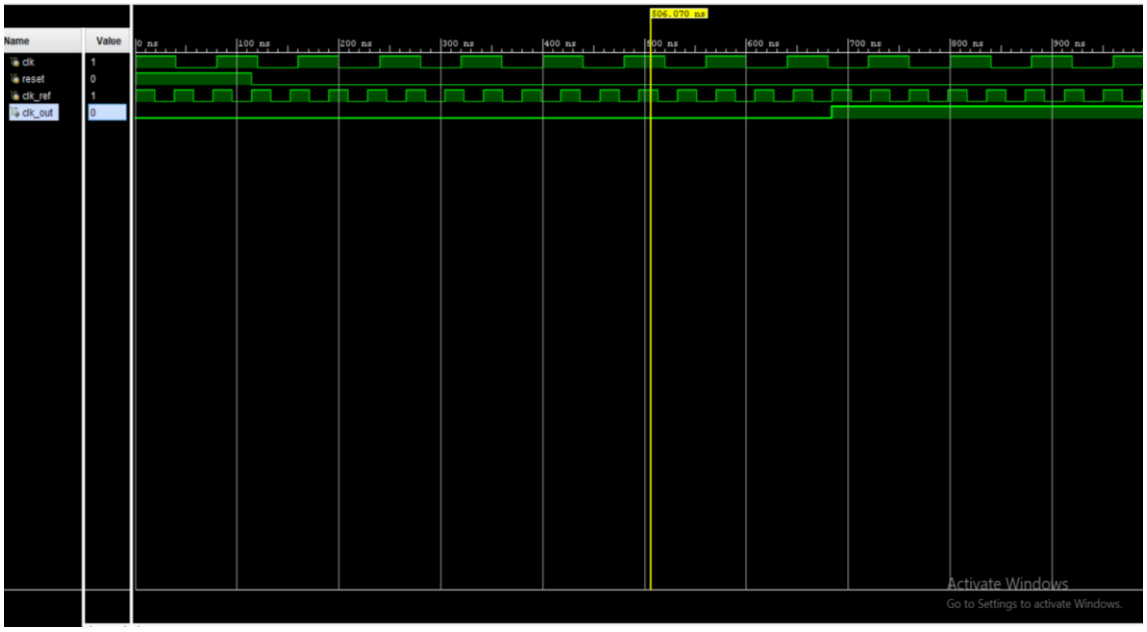

Figure 3: Results of proposed architecture

Figure 3 shows the simulation of the proposed design. The output shows improvement as compared to the other results.

IV CONCLUSION

Among variety of frequency synthesizers' fractional N PLL frequency synthesizers have the capability of giving high performance using low power and low chip area. This is done by using Xilinx tool. Since it is made of several individual blocks each block is designed separately and analyzes their power consumption and all blocks are connected to achieve a power efficient PLL frequency synthesizer. The goal here is to achieve a PLL frequency synthesizer which is capable of giving wide range of frequencies and to achieve this, choose the components that are best suited. Micro-wind software has been used to verify our design that is implemented by using Xilinx tool. Many references have been considered and the best technology among them has been chosen to implement the Power efficient phase locked loop filter frequency synthesizer with low chip area and low phase noise and high speed.

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