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A System Parameter Analysis of Linear Techniques For CMOS Transconductor

Sandeep Bansal*, Ankit Chaudhary

School of Electronics and Electrical Engineering

Lovely Professional University, Punjab, India

*sandeep.15732@lpu.co.in

Abstract: The present article illustrates the design and parameter analysis of different configuration used for linear MOS voltage to current conversion (transconductance) with wide linear input range. Operational transconductance amplifiers (OTA) has been most significance block in analog circuits. The trend in modern wired as well as wireless communication system is to achieve higher data rates and higher bandwidth and high linearity in analog front end circuits and analog filters. We have summarized the performance of different techniques. Large linear range is achieved in lower process technology.

Keywords: MIFG-MOS, ARDP, HD, OTA, MOSFET, Gm-C, DVD.

I. INTRODUCTION

Transconductor is a basic circuit in analog environment based circuit application such as filter design gain amplifier, sigma delta modulator and interface circuits [1]. The main application of the transconductor is to exchange the applied voltage signal into current signal at output terminal, transconductor based circuit is usually called Voltage-Current converter. There is a requirement of high transconductance and good controllability in lower time period continuous time filter and the used OTA filter should provide high transconductance and good controllability. While RC filter provides constant cut-off frequency irrespective of input signal variation. The OTA is prerequisite good linearity in the entire range of input signal. Good linearity related to that OTA must have constant Gm, graph in his input limit [3]. The linearity during the voltage-to-current conversion should usually preserve because the linear range of transconductor govern the linearity of whole system. Now a day the challenge is that the power supply and size of the device is scale down to achieve more speed because of this linearity create problem to achieve sufficient signal level [1]. Most of transconductor

ISSN: 0971-1260
Vol-22-Issue-16-August-2019

application system requires low noise and current consumption along with good linearity over a significant range. In transconductor due to differential structure even harmonics does not exit but odd harmonics play a vital role in the distortion of the output current [2]. Types of Linearization Techniques; Source Degeneration (Either Resistor or MOS) [5], Cross Coupled Differential Pair, Adaptive Biasing, Mobility Compensation Techniques [3], Shift Level Biasing [4], Input Signal Attenuation, Transconductor Employing Body Effect, Transconductor Utilizing Squaring Circuit.

Source degeneration gives good linearity but there is a trade-off comes in consideration between space and reduced common mode rejection ratio. The two source degenerated differential pair could be used to terminate harmonic distortion. The Pseudo- differential arrangements could accomplish good linearity because absence of tail current source [12, 13]. But these structures have poor common mode rejection ratio so we have to employ extra circuitry to achieve desired performance. Analog filter designed using different methodologies: Discrete Time filter design, Switch Capacitor based filter design; Switch Current based filter design, Continuous Time implementation [11]. Due to sampling process we cannot use Switched Capacitor, Switched Current at lower time interval. Continuous time filter have a high speed as compare to discrete filter because absence of sampling process in Continuous filter. There are three main procedures to implement filter [11]. Active Resistive Capacitor Filter, MOSFET-Capacitor Filter, Transconductance (Gm) – Capacitor Filter. Active RC filter use passive frequency element like as op-amp, resistor, capacitor, they provide worthy linearity but prerequisite large die area, tuning could accomplished by placing arrays of passive component. MOSFET-C [5, 6] active filter has deprived linearity because of non-linear behaviour of CMOS transistor. Linearity could be upgraded by placing manifold Cross Combined transistor [7], and input active range is compact in demand to preserve the MOSFET in linear region. Gm-Capacitor configuration [8], [9] has stable frequency reaction in respect to active Resistor Capacitor, MOSFET- Capacitor, because of nonappearance of feedback to the active elements. Gm-Capacitor has poor linearity. But noise and linearity are in a trade-off situation in this filter. There are different types of Gm-c filters are implemented now a days, such as first order, second order etc. With an improved version of Gm-c, its performance also increases [16].

II. LINEAR TECHNIQUES

ISSN: 0971-1260
Vol-22-Issue-16-August-2019

A. Simple MOS Transistor

The simplest CMOS transconductor with differential current tail pair is show in Figure 1. The input is given to the gate terminal of the MOS transistor and current is applied at the drain terminal of both the transistors. We assume that the both the transistor is working in the strong inversion operation.

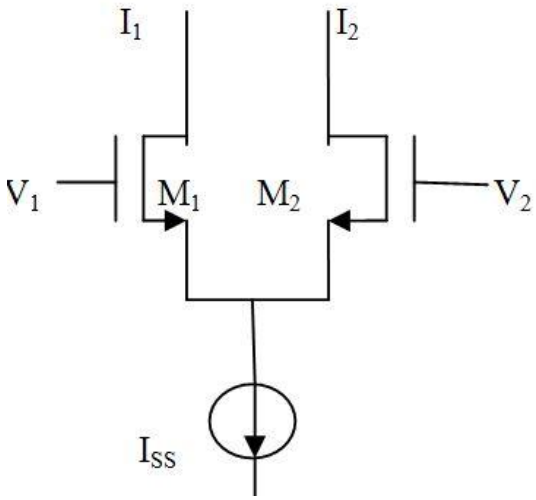

Fig 1: Simple CMOS transconductor [1]

The transfer function of this basic transconductor is specified as [1]

$$I_{out} = I_1 - I_2 = G_{mo} V_{id} \sqrt{1 - \frac{\beta_{1,2}^2 V_{id}^2}{G_m^2}}$$

where

$$V_{id} = V_1 - V_2$$

$$\beta_{1,2} = 1/2 \mu_0 C_{ox} (W/L)$$

and

$$G_{mo} = \sqrt{2 I_{ss} \beta_{1,2}}$$

$\beta_{1,2}$ and G_{mo} are respectively transconductance ratio and transconductance of transistor $M_{1,2}$. As V_{id} cross the certain value the entire polarization current pass through the one transistor and turned off the other transistor. The maximum value of the V_{id} is specified as:

ISSN: 0971-1260
Vol-22-Issue-16-August-2019

$$V_{id,\max} = \sqrt{2}\frac{I_{ss}}{Gmo}$$

So from this equation we can say that for a particular I_{ss} current the liner range can be stretched by sinking the transconductance $M_{1,2}$. Source degeneration resistor is a common technique to decrease the transconductance [1]. This source degeneration resistor upturns the supply voltage at the source terminal so decrease the drain current. But for a significant decrease in value of transconductance we need a large value of resistor which is unavailable in the majority of CMOS technology [15].

B. MULTIPLE INPUT FLOATING GATE (MIFG) CMOS TECHNIQUE

MIFG MOS is used in corresponding to the source coupled pair. The region of operation of MIFG MOS should be strong saturation operation. The given circuit is shown in figure 2.

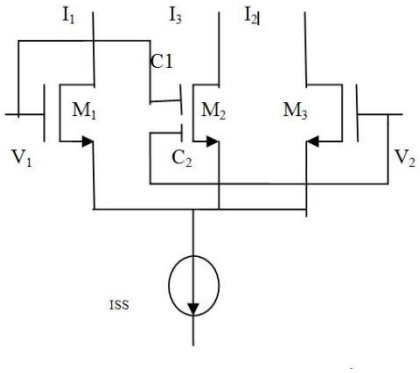

Fig 2 : MIFG MOS Transconductor[1]

The transfer function of this circuit is given below

$$I_{out} = \left(\frac{2\beta_{1,2}}{1+\frac{\beta_3}{\beta 1,2}}\right)\left(\sqrt{1-\frac{\beta_{1,2}V_{id}^2}{G_{mo}^2}}\right)V_{id}$$

$$I_{out} = \frac{G_{mo}}{A}V_{id}\left(\sqrt{1-\frac{\beta_{1,2}^2V_{id}^2}{G_{mo}^2}}\right)$$

Where A is given as geometrical size of M_2 and $M_{1,2}$

$$A = \sqrt{1+\frac{\beta_3}{2\beta 1,2}}$$

The MIFG MOS circuit simulated in a double poly .8µm CMOS technology. Voltage supply is 3V and the bias current 10A, and size of transistor $M_{1,2}$ to $(W/L)_{2,1}$ = (10µm/4µm). The maximum linearity was achieved for (W/L) = (88µm/4µm). We see that the linearity directly

ISSN: 0971-1260
Vol-22-Issue-16-August-2019

depend upon the value of A. Higher the value of A higher will be linearity. So for good linearity value of A should be as large as possible.

C. ATTENUATED RESISTOR DEGENERATED DIFFERENTIAL PAIR (ARDP) TECHNIQUE

This linearization method employ an attenuator monitored by source degenerated operational transconductance amplifier. Degeneration may be two type either it can use a MOS or resistor in triode range of operation.

The circuit of OTA (ARDP) is given in figure 3 below:

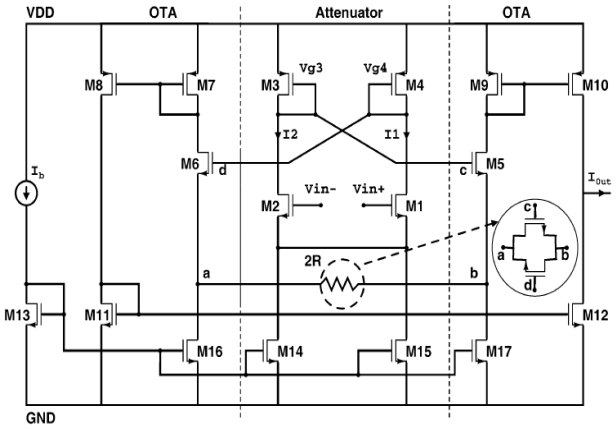

Fig 3: OTA (ARDP)

The attenuator fundamentally the differential attenuator with diode coupled PMOS load transistors. In this circuit attenuator output work as an input for source degenerated OTA [2].

$$I_1 = \frac{I_b}{2} + \frac{1}{2}\sqrt{2\beta_n I_b} * \mathrm{V}_{id} - \frac{1}{8}\sqrt{2\beta_n I_b}(\beta_n / I_b) * \mathrm{V}_{id}^3$$

$$I_2 = \frac{I_b}{2} - \frac{1}{2}\sqrt{2\beta_n I_b} * \mathrm{V}_{id} + \frac{1}{8}\sqrt{2\beta_n I_b}(\beta_n / I_b) * \mathrm{V}_{id}^3$$

$$\Delta V_g = V_{g3} - V_{g4} = \sqrt{\frac{I_1}{\beta_p}} - \sqrt{\frac{I_2}{\beta_p}}$$

$$V_g = \frac{V_{id}}{\sqrt{m}}$$

ISSN: 0971-1260
Vol-22-Issue-16-August-2019

$$m = \frac{\beta_p}{\beta_n} = \left(\frac{\mu_p}{\mu_n}\right)\left\{\frac{(W/L)_{p3,4}}{(W/L)_{n1,2}}\right\}$$

Where m is proportion of transconductance factor of the load transistor to input transistor called attenuation factor. Some non-linearity is still exit because of mobility degradation, idealities problem of transistor, second order effects.

At this instant this differential voltage is given at input of resistor degenerated OTA. The output current of this OTA is given below [2]:

$$I_0 = \frac{\sqrt{2\beta_n I_b}}{\sqrt{m}(1+N)} * V_{id} - \frac{1}{4m^{\frac{3}{2}}(1+N)^{\frac{5}{2}}}\sqrt{2\beta_n I_b}(\beta_n / I_b) * V_{id}^3 \quad (11)$$

$$G_m^{'} = \frac{\sqrt{2\beta_n I_b}}{\sqrt{m}(1+N)}$$

$$HD_3^{'} = \frac{1}{32}\frac{V_{id}^2}{m(1+N)^2(V_{GS}-V_{th})^2}$$

It is clear that if the value of m will increase than the harmonic distortion will be decrease as well as increase the value of linear range. But there is limitation on the value of m, we cannot increase the value of m after certain limit. Higher value of m decrease the voltage swing at the output and force the load transistor enter into sub-threshold region.

This circuit was implemented under .18μm CMOS technology under 1.8V power supply. It shows the common mode rejection ratio(CMRR), power supply rejection ratio(PSRR) - 60 dB and -58 dB respectively. Input noise spectral noise density 70nV for 10 MHz frequency. In this -70 dB HD3 is attained for 600mV with a linear range of 1.2V peak to peak for 1% transconductance.

D. A Noval CMOS OTA Based On Mobility Compensation Procedure

To remove the mobility effect Coban and Allen provide a configuration in which they practice of parallel grouping of linear and saturation devices [3]. Even though the circuit indications a worthy linearity, circuit input range was not adequate for application such as video application circuit. Then a new approach makes use of triode and subthreshold region transistor. Parallel arrangement of linear and subthreshold region transconductor could cancel

ISSN: 0971-1260
Vol-22-Issue-16-August-2019

harmonics term. And this could lead to the rise the linearity property. Transistors M_{N3}-M_{N4} operates in sub-threshold region. Third order harmonics terms of linear and sub-threshold region has reverse signs.

The output current is specified as [3]

$$I_{out} = I_1 - I_2 = (I_{mn1} - I_{mn2}) + (I_{mn3} - I_{mn4})$$

Mobility compensation techniques based circuit is shown in figure 4.

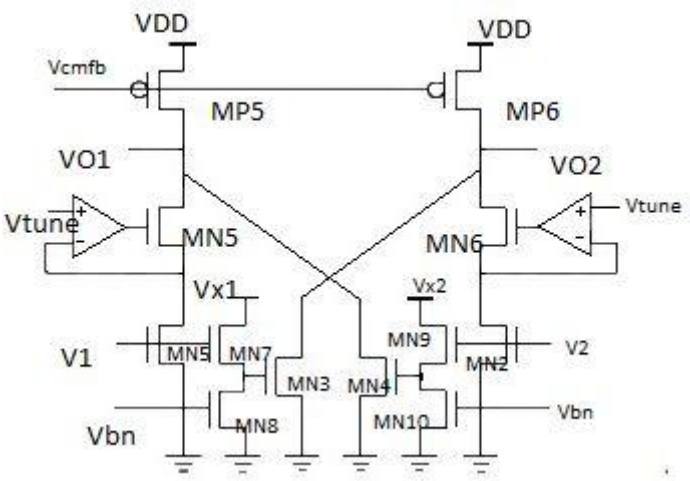

Fig 4: Mobility compensation based OTA

The drain current in MN3 and MN4 given as

$$I_{mn3} = \beta_3 V_t^2 (\eta - 1) e^{(V_{GS3} - V_{THN})/\eta V_t} \left(1 - e^{-V_{DS3}/V_t}\right)$$

$$I_{mn4} = \beta_4 V_t^2 (\eta - 1) e^{(V_{GS4} - V_{THN})/\eta V_t} \left(1 - e^{-V_{DS4}/V_t}\right)$$

The triode region G_m is deviated to the +ve sign whereas the linear G_M have -ve sign, with a better parallel arrangement of these two Gm we acquire the over-all G_m having a improved linearity and a broader input limit for a defined limit of error. Subsequently the input operating limit of OTA is exaggerated by V_B and $A_{v,sf}$ these twofold design parameter should be wisely selected to promise M_{N3}, M_{N4} to operate in the subthreshold region.

If V_B has too large the gate source voltage of M_{N3}, M_{N4} are excessively large, transistor dimension to conserve the recompense capability should be engorged to a disagreeable value. For large Av as the input increase, there exit the region that M_{N3}, M_{N4} modify his operation sub threshold region to saturation region and OTA has lost his compensation capability.

ISSN: 0971-1260
Vol-22-Issue-16-August-2019

Here the source follower circuits play an important role to determine the optimum value of $A_{v,sf}$ and V_B. The circuit suffer G_M variation because of process parameter mismatch. This circuit has ± 0.5% Gm deviation in the wide input range of ± 0.8V. The THD is under -60 dB. A 9th order Bessel-Filter for a DVD read channel equalizer using this OTA was simulated with 0.35-μm n-well CMOS process. This circuit indicate the cut-off frequency of 8-MHz and group delay ripple is less then ±2.1% over the range from .5fc to 2fc. Filter use about 65mW power under at 3.3V supply [3].

E. Transconductor Using Body Effect for Low Frequency Application

In this techniques problem of narrow input range of the transconductor in medical devices, which has low frequency can be eliminated by an improved local-feedback MOS transconductor operating in sub-threshold region utilizing body effect. Newton Raphson and Downhill Simplex method is used in the designing of this transconductor [14]. The biological signal frequency is several hundred hertz and the magnitude is 1μV to 100mV [10]. For the low frequency application the time constant values should be higher. For a 100Hz frequency transconductor should be less than 1μS.

Nonlinearity can be compensated by change the threshold voltage with the help of body voltage. Threshold voltage is given as:

$$V_{th} = V_{tho} + V_{OFF} + \gamma\left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}\right)$$

$$\Delta V_{th} = \gamma\left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}\right)$$

V_{th} ,V_{OFF}, γ, V_{SB} , ΔV_{th} are the threshold voltage of a transistor operating in strong inversion region, when VSB=0 , the offset threshold voltage of a transistor operating in sub-threshold region, body effect coefficient, the Fermi-potential the source bulk voltage, and the variation of the threshold by body effect respectively. If the value of V_{SB} is decrease then the value of drain current will be increase. The schematic is shown in figure 5 below:

ISSN: 0971-1260
Vol-22-Issue-16-August-2019

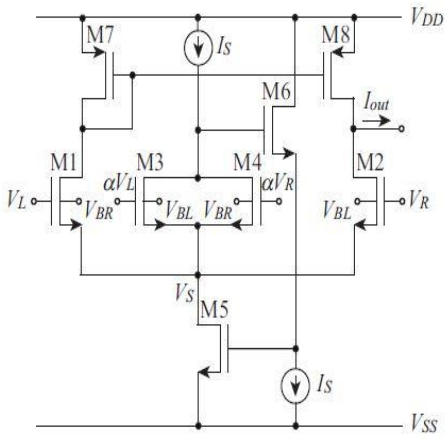

Fig 5: Low Transconductance circuit using body effect [4]

To reduce the nonlinearity of the improved LFB OTA the common source voltage VBL and VBR of the active voltage divider are used for the bulk voltage of the proposed transconductor [14]. In the simulation of this circuit design .18μm BSIMS model is used. The supply voltage is ±.9V. The THD around -40dB for input voltage magnitude 170mV and the frequency of input voltage 100Hz. Power consumption at Gm = 1μS is 682nW.

F. Squaring Circuit Based Linear Transconductor

This technique based circuit is able to tune by adjusting the bias voltage. This circuit shows the significant application for highly linear continuous time filter. Voltage tunable transconductor linearization method based on a bias offset technique which provide a high linearity and consume low power. Transistor M6 – M7 form the differential pair, while transistor M1- M4 constitute the bias offset transconductor. This squaring circuit provide the input independent bias current to differential pair in such a different way that M5 and a current sink I0 are used to level shift the summed the drain current of IL and IR from vertex A to vertex B. the drain current of the transistor M6 and M7 are id1 and id2 is expressed as:

$$I_{D1} = K_n\left(-\frac{Vid}{2} + V_M - V_S - V_T\right)^2$$

$$V_S = -\frac{1}{2}\sqrt{\frac{I_{SS}}{K_n} - V_{id}^2 - V_B^2} - \frac{V_B}{2} - V_T$$

ISSN: 0971-1260
Vol-22-Issue-16-August-2019

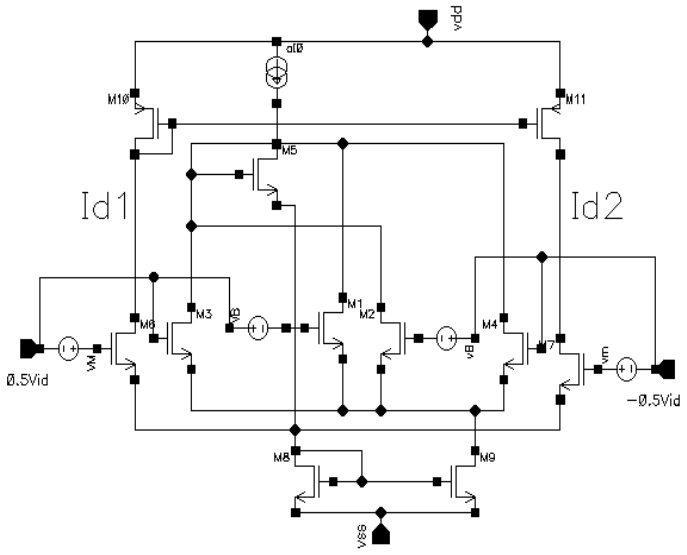

Fig 6: Linear Transconductor Using Bias Offset Scheme

The saturation condition of transistor is

$$V_{id} > 2\left(-V_M + V_S^{'} + V_T\right)$$

$$V_{id} < 2\left(V_M - V_S^{'} - V_T\right)$$

Where

V_T is the threshold voltage of n- channel MOS transistor.

$$V_M \cong V_S^{'} + V_T$$

$$I_{SS} = K_N V_{id}^2 + 4I_o$$

$$I_{SS} = \frac{1}{4} K_N V_{id}^2 + I_o$$

Putting values of I_{SS} and V_S

$$V_S = -\frac{1}{2}\sqrt{\frac{K_N V_{id}^2 + 4I_o}{K_n} - V_{id}^2 - V_B^2} - \frac{V_B}{2} - V_T$$

$$V_S = -\frac{1}{2}\sqrt{\frac{4I_o}{K_n} - V_B^2} - \frac{V_B}{2} - V_T$$

ISSN: 0971-1260
Vol-22-Issue-16-August-2019

Above equation show that V_S is independent of V_{id} and show the linear characteristics.

The circuit shown in figure 6 is implemented in Cadence VIRTUOSO atmosphere of UMC .18um CMOS method machinery operated with 27°C with V_T = .523V.The DC voltage gain is 5.29 DB and the bandwidth of 1.69 GHz. The linear range was within -62V to .54V.

G. Linear MOS Transconductance with Source Degeneration and Adaptive Biasing

1. CMOS Transconductor with Resistive Source Degeneration

In Resistive Source Degeneration techniques V-I characteristic for MOS transistor in the saturation region and the second order effect ignored for straightforwardness. The circuit diagram of resistive source degeneration based transconductor is shown below [11].

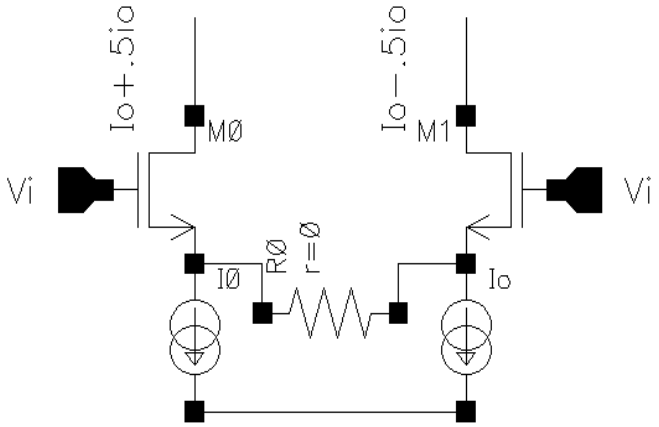

Fig 7: CMOS Transconductor Based On Degeneration Resistor

Drain current is given by:

$$I_D = \frac{\beta}{2}\left(V_{gs} - V_t\right)^2$$

In this circuit better linearity achieved for large gate to source voltage but for low gate to source voltage this gives poor linearity. We can solve this problem by using degeneration resistor but this will require large value of resistor to attain an extensive linear input limit. Given method removes tuning capability because this value is decided with the help of resistor.

ISSN: 0971-1260
Vol-22-Issue-16-August-2019

2. Source Degeneration Method Based CMOS Transistor

In this techniques substitute resistor with two CMOS transistor working in the linear region of operation as shown in figure 8.

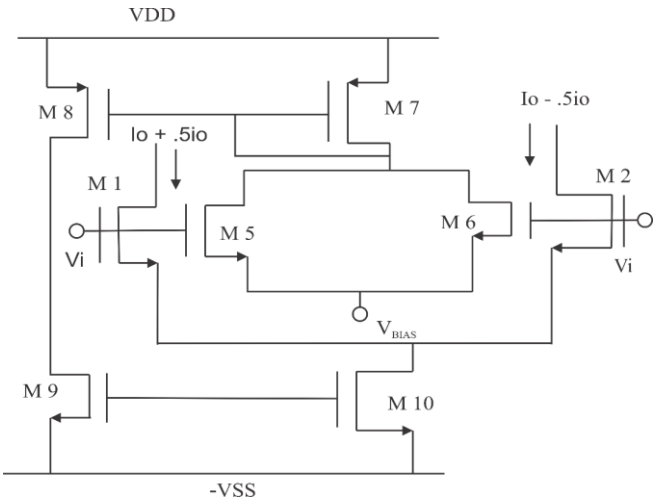

Fig 8: Source Degeneration Method Based MOS Transistor

Here M1-M2, M3-M4 should be perfectly matched and neglect second order effect. Transfer characteristic of this circuit is given is given as:

$$I_o = \frac{\sqrt{2\beta_1 I_o}}{a} V_i \sqrt{1 - \frac{\beta_1 V_i^2}{a^2 I_o}}$$

Where

$$a = 1 + \frac{\beta_1}{4\beta_3}$$

Non-linear value below the square root have to made far lesser compare to unity and enhanced linearity and we can obtain superior input dynamic limit.

3. Adaptively Biased MOS Transistor

In this technique a tail current having an input reliant on quadratic component for terminate the nonlinear term only when $I_o = I'_o + \frac{\beta V_i^2}{8}$

ISSN: 0971-1260
Vol-22-Issue-16-August-2019

According to technique nonlinear transfer characteristic should transform into linear ones, tail current I_0 must have the same value $I_o = I'_o + \frac{\beta_1 V_i^2}{8a^2}$

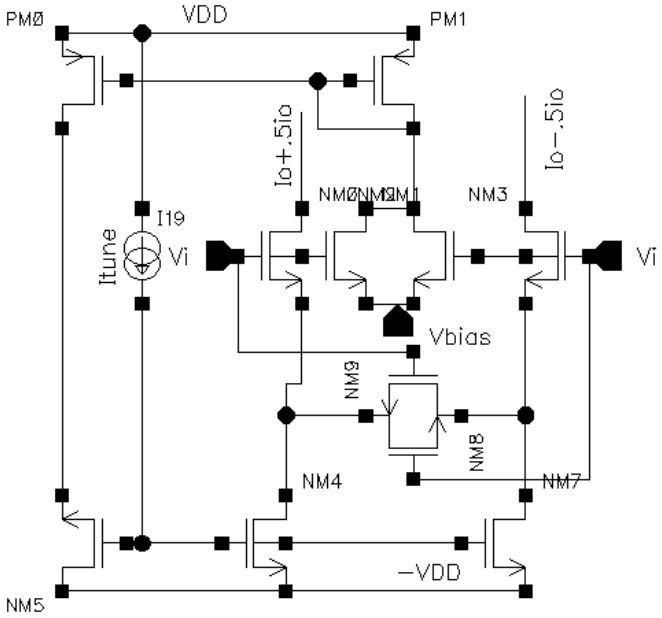

Fig 9: MOS transconductor based on Source Degeneration and Adaptive Biasing

This circuit shown in figure 9 is implemented in .35µm CMOS under a single voltage supply of 3.3V. The entire transconductor dissipates 1mW for Gm=40µS and 5-MHz bandwidth. The circuit shows the good linearity for fully balanced as well as unbalanced output. Table 1 summarizes the parametric comparison of various techniques.

Table 1: Parametric comparison of different techniques

Techniques	**Supply voltage**	**THD/ HD3**	**Process**	**Power Consumption**	**Linear range (Vpp)**
MFG MOS	3V	-	.18µm CMOS	-	.8V
ARDP	1.8V	-7dB	.18µm CMOS	-	1.2V
Mobility Compensation	3.3V	-6dB	.35µ n well CMOS	65mW	.8V
Source degeneration Adaptive biasing	3.3V	-	.35µ CMOS	1mW	1V
Body effect	0.9V	-40dB	.18µm BSIMS	10mW	100mV

ISSN: 0971-1260
Vol-22-Issue-16-August-2019

III. CONCLUSION

Centred on the literature review the following gaps in the study of linear transconductor and analog circuits design based on transconductor application have been listed as, Different practices have been recommended to improve the linearity of the transconductor but in low-voltage applications the non-linearity problems exist in many transconductor circuits. Researchers have reported Total harmonic distortion (THD) of the transconductance circuits, but there is a possibility to reduce this factor to the lower values. For the use of the linear transconductor in the designing of Gm-C filters, the there is a trade-off between bandwidth and intrinsic gain when selecting MOS drain current, inversion level and channel length. In previous years the more attention of research is given to improve the linearity of the transconductor. But very less importance is given to the noise analysis of the transconductance. If we introduced linearization methods there will be appear extra nodes in circuit generating parasitic poles and zeros and hence there is degradation at high frequency application.

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ISSN: 0971-1260
Vol-22-Issue-16-August-2019

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