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Comparative Study of Si-Nanowire Fetand Tunnel-Nanowire FET

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***Abstract:*-Nanowire FET devices are one of the alternative semiconductor devices which have potential to replace the existing MOSFET technology in future. In this paper a comparative study of Si nanowire FET and Tunnel nanowire FET with respect to electronic properties is reported.In devices metallic contacts are considered as source and drain as well as Si nanowire is considered as a channel between source and drain. Different simulations are performed in nanoHUB as well as TCAD tool with different channel length to analyze the impact of different factors on electronic transport inside the nanowire FETs. Analysis are observed with the scaling the channel length of both the nanowire FETs. It is observed through simulation results that at low gate voltage, drain current and the sub-threshold swing increases.**

Keywords: MOSFET, NW-FET, TFET, oxide-thickness, threshold-voltage, channel-length.

INTRODUCTION

In MOSFET (metal oxide semiconductor field effect transistor) technology, generally two device structures are studied widely, the first one is bulk structure and second one is silicon on insulator (SOI). In bulk structure any transistor is fabricated directly on the substrate of semiconductor whereas in SOI transistor is fabricated on thin layer of silicon and it is separated with a layer of insulator from the substrate. The bulk process of manufacturing the MOSFET is relatively simple and is widely adopted by the semiconductor industries. According to ITRS device scaling is important factor to achieve the goal of semiconductor industry, but scaling beyond 20 nm is quite complicated to maintain all the device parameter further [1-3]. So many efforts are going on parallel to replace the existing MOSFET technology worldwide. In scaling functionality and reliability of the device has to maintain at small dimension, because of this activity short channel length comes into the pictures along with some other parameters. Effect of this causes the reduced sub-threshold swing which further causes to difficulty in turn on the device.

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Vol-22-Issue-16-August-2019

In nano-regime many devices such as FinFET, DG-FET,Tunnel-FET, CNTFET, Nanowire-FET, Organic-FET etc. has capability to replace the existing MOSFET technology but still research are going on for mass production [4]. Tunnel-FET and Si-Nanowire FET has immerges as a potential candidate for future devices.

DEVICE STRUCTURE

As compared to MOSFET, nanowire FET devices also control the current flow from source to drain through the gate voltage and simultaneously turned on and turned off the device [5-7]. Regarding electrostatic property of channel, due to channel of the device is surrounded by the gate, as shown in Fig. 1, the nanowire FET device can control electrostatic of channel better than the existing MOSFET device.

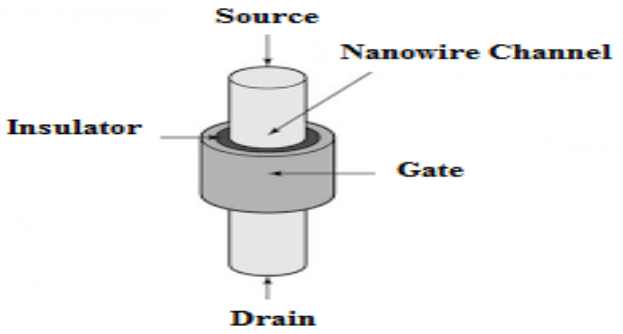

Fig.1. Schemetic of Nanowire FET

As compare to MISFET device, nanowire FET is having source/drain, gate-oxide , gate, channel, spacer and extension. All the components are manufactured in the shape of tube through different implantation method [8]. Channel of the device is controlled by inner as well as outer gate (Fig. 2). Outer gate of the device is acting as a gate-all-around whereas inner gate is working for enhanced charge-control.

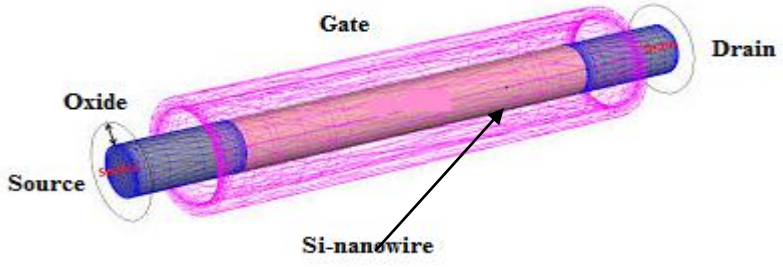

Fig.2. Schemetic of Si-Nanowire FET

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In short-channel FET device some portion of depletion is due to source and drain bias whereas in long-channel FET device gate is fully responsible for the depletion of semiconductors ions. In present scenario scaling means the reduction in channel length, but as we follow this technique in nano regime the leakage current increases drastically, which is one of the prime concerned [9-11]. Out of so many proposed devices the nanowire FET device has attracted researches because of its potential to replace the existing MOSFET technology [12-14].

Result analysis of Si nanowire-FETdevice

Silicon (Si) is widely available material in the Earth, whereas the crystal (Fig.3) of silicon structure is highly stable. Because of good electrical and mechanical properties of Si material it is best suitable for semiconductor industry [14-18]. SiO2 is a native oxide of Si which is widely used as insulator in the in semiconductor devices.

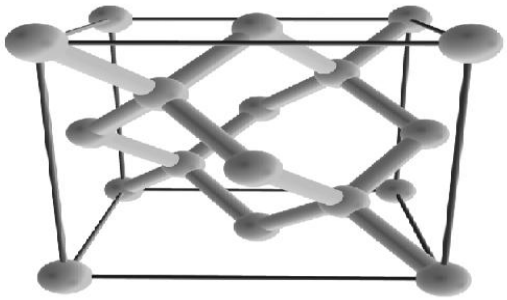

Fig. 3. Cross view of Silicon structure

For simulation of Si nanowire FEt device, the length of source and drain are fixed to 10nm and the channel length is in range of 12 to 4 nm. Other parameter like oxide-thickness of the device as well as the diameter of the nanowire are considered as 2.5nm and 1 nm respectively. Doping concentration of 2e+20/cm^3 is considered for donor,source and drain doping concentartion, whereas 1e+06/cm^{3}is fixed for acceptor, source and donor concentration.

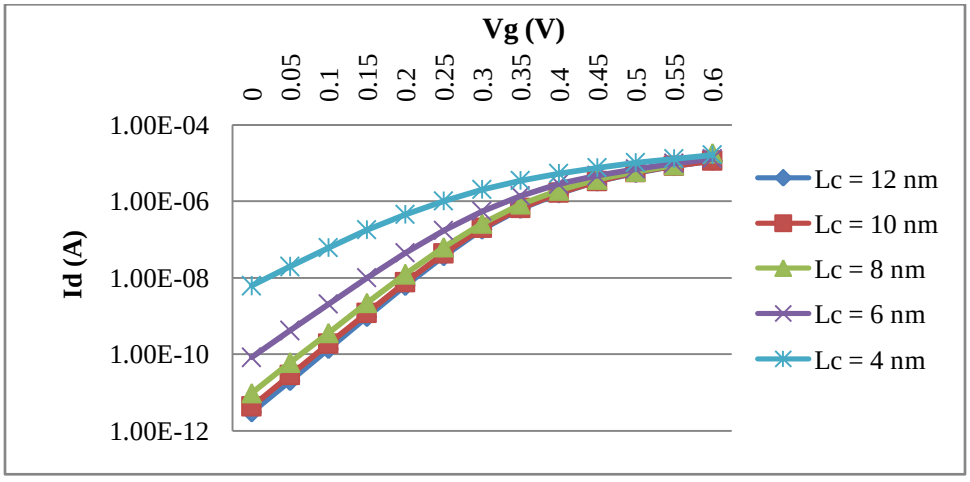

Fig.4. I-V plot for Si- nanowire FET device

ISSN: 0971-1260
Vol-22-Issue-16-August-2019

Result analysis of Tunnel nanowireFET device

A p-i-n structure is present in TFET device where source is p-doped, drain is n-doped and channel is intrinsic as shown in Fig. 5. The intrinsic part in form of channel is completely covered by the gate electrode whereas the mechanism of switching depends upon the band-to-band tunnel phenomenon [19-20].

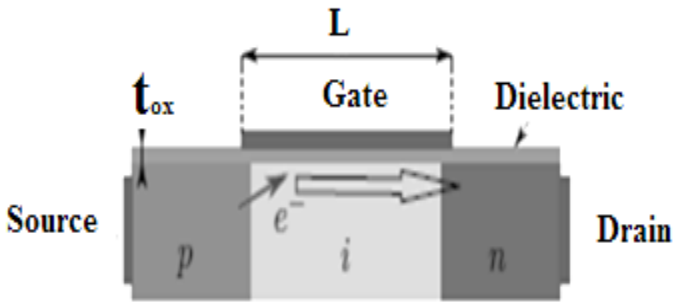

Fig.5. Schematic of Tunnel FET device

In Tunnel FET device, at off state band-gap of source, drain as well as channel prevent the flow of current which results, minimum current leakage in off state. At on state band-to-band tunneling leads to inject the holes from source side towards the channel.

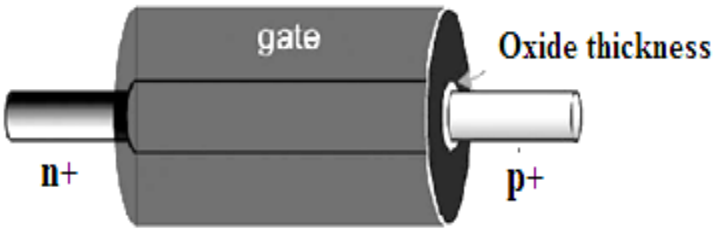

Fig.6. Schematic of Tunnel Nanowire-FET device

Tunnel NW-FET as shown in Fig. 6, the channel dielectric is considered as 11.9whereas affinity of channel-material is considered as 4.24 eV. In device work function of gate contact as well as the insulator's dielectric constant is considered as 4.26 eV and 3.9 respectively.

In Fig. 7, impact of gate voltage on drain-current with variable channel length from 12 to 4 nm is shown. For simulation the total length of the device is considered as 32 nm.

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Vol-22-Issue-16-August-2019

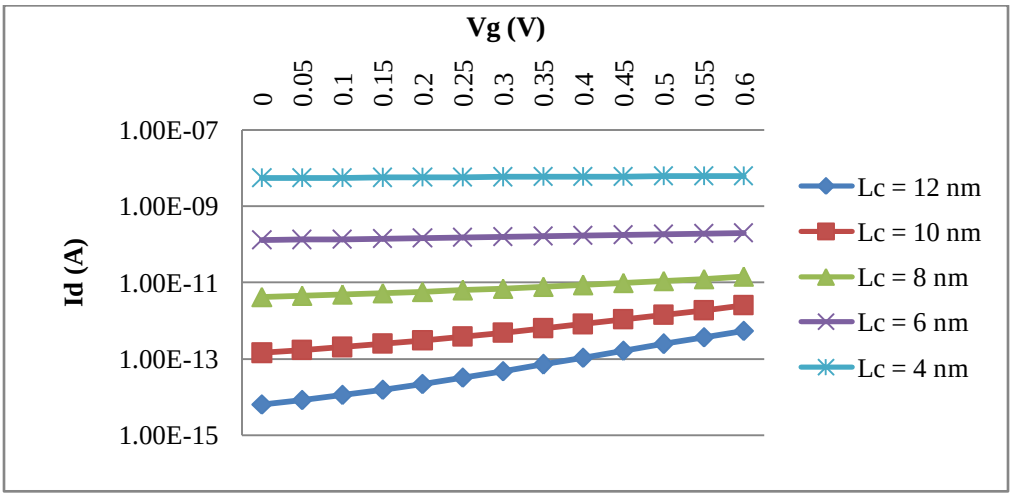

Fig.7. I-V plot for Tunnel nanowire FET device

CONCLUSION

In nanometer regime nanowire FET devices have some promising characteristics which will lead a potential candidate for future semiconductor device. A new class of devices is represented by nanowire FET and tunnel FET. This paper is focused to the electronic-transport of silicon nanowire FET and tunnel nanowire FET with variable channel length. The simulation results shows that while reducing the channel length of the nanowire FET device, a substantial increment in sub-threshold swing and drain current is observed at low gate voltage, which on is very important for nanometer devices.

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