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Comparative Performance Analysis of Low Offset High Speed CMOS Voltage Comparator

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Abstract

This paper presents comparative performance analysis of Low Offset High Speed Voltage Comparators. High speed applications and technology is becoming an increasingly important and growing area of electronics. Various types of dynamic latch comparators which include resistive dividing comparator; current sensing comparator; charge sharing comparator and modified high speed CMOS Voltage Comparator simulated for the different characteristics in generic 90 nm CMOS Technology. In modified comparator design an attempt has been made to reduce the offset error generated within the latched comparator by introducing Offset Reduction Block.

Keywords:

Comparator, CMOS, Propagation delay, Offset Voltage, Power Dissipation, Differential Current Sensing Comparator, Charge Sharing Dynamic Latch comparator

1. Introduction

The schematic symbol and basic operation of a voltage comparator are shown in figure 1. The comparator can be thought of as a decision making circuit.

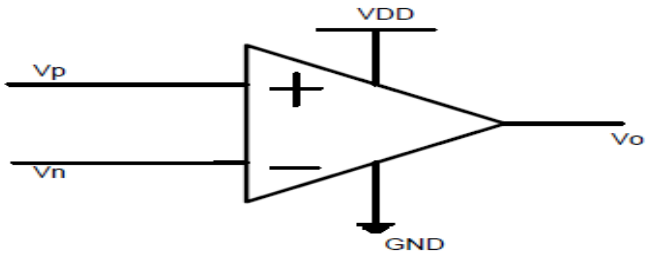

Figure 1. Circuit Symbol for a Comparator

The comparator is a circuit that compares an analog signal with another analog signal or reference and outputs a binary signal based on the comparison. V_P is the input voltage applied to the positive input terminal of comparator and V_N is the reference voltage applied to the negative terminal of the comparator. If the V_P, the input of the comparator is at a greater potential than the V_N, input, the output of the comparator is at logic 1 where as if V_P is at potential less than V_N the output of the comparator is at logic 0.

If $V_P \geq V_N$, then Vo = logic 1.

If $V_P < V_N$, then Vo = logic 0.

The comparators can be classified into open-loop and regenerative comparators. The open-loop comparators are basically op-amps without compensation. Regenerative comparators use positive feedback, like sense amplifiers or flip-flops, to accomplish the comparison of the magnitude between two signals. A third type of comparator emerges that is a combination of the open-loop and regenerative comparators. This combination results in comparators that are extremely fast.

The Comparator is the main building block in ADC architecture. Comparators are known as 1-bit analog-to digital converter and for that reason they are mostly used in large abundance in A/D converter. The accuracy of such comparators, which is defined by its offset, along with power consumption, speed is of keen interest in achieving overall higher performance of ADCs.

A comparator has a binary output whose value is based on a comparison of two analog inputs. This is illustrated in Figure 2. The output of the comparator is high (V_{OH}) when the difference between the non-inverting and inverting inputs is positive, and low (V_{OL}) when this difference is negative. Even though this type of behavior is impossible in a real world situation, it can be modelled with ideal circuit elements with mathematical descriptions. One such circuit model is shown in Figure 3, comprises a voltage-controlled voltage source (VCVS) whose characteristics are described the mathematical formulation given on the Figure 3.

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2. Existing Architectures of Comparator

Open-loop, continuous time comparators, are an operational amplifier without frequency compensation to obtain the largest possible bandwidth, hence improving its time response. Since the precise gain and linearity are of no interest in comparator design, no-compensation does not pose a problem. However, due to its limited gain-bandwidth product, open-loop comparators are too slow for many applications. One the other hand, a cascade of open-loop amplifiers usually has a significantly larger gain bandwidth product than a single-stage amplifier with the same gain. However, since it costs more area and power consumption, cascading does not give practical advantages for many applications.

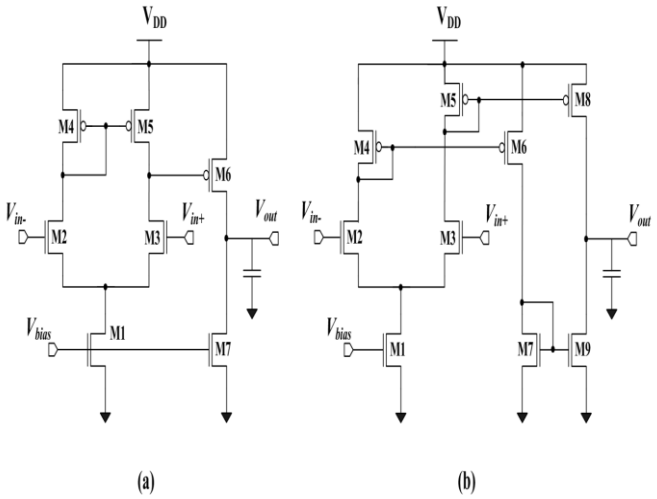

Figure 6. (a) Two-stage open-loop comparator
(b) Push-pull output open-loop comparator

Figure 7. Shows typical types of pre-amplifier based latched comparators. The main advantages of the pre-amplifier based latched comparators are their fast speed and low input referred latch offset voltage. Typically, pre-amplifier, which consists of one or two stages of an open-loop comparator, has a gain of 4 - 10 V/V and it can reduce the input referred latch offset voltage by its gain. For example, if a pre-amplifier has gain of 10 V/V and a latch stage has an offset voltage of 50mV, then the input-referred latch offset voltage will be 5 mV. In addition, by using pre-amplification stage, kickback noise can be considerably reduced (by isolation between the drains of the differential pair transistors and the regeneration nodes) and meta-stability problem also can be relaxed.

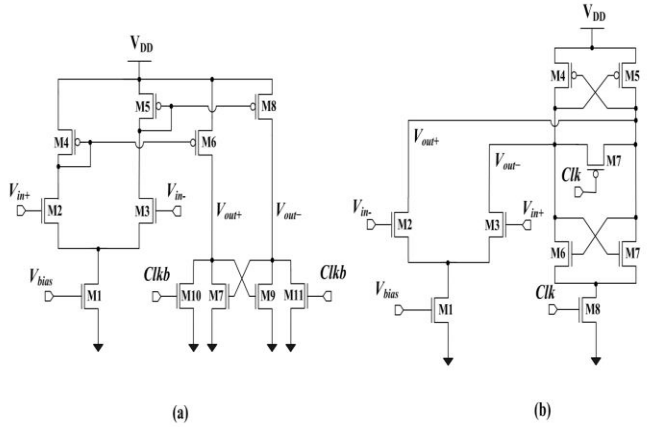

Figure 7. (a) A static latched comparator [13] (b) A class-AB latched comparator [13-14]

Latched comparators commonly employ one or two clock signals (Clk and Clk_b) to determine the modes of operation: Track Mode (Reset): output is reset, and input is tracked, Latch Mode (Evaluation): output is toggled by using a positive feedback. For the operation of the circuit shown in Figure 7 (a), during reset phase (Clk_b=0V), both complementary output V_{out}+ and V_{out}− are reset to 0V by reset (switch) transistor M10 and M11. During evaluation phase (Clkb=V_{dd}), as the reset transistors are off, the comparison will be performed by a positive feedback from transistor M7 and M9. While this comparator present low kickback noise, relatively large static power consumption and slow regeneration due to its limited current operation make it less attractive. Similarly, the operation for the circuit shown in Figure 7 (b)during reset phase (Clk=0V), PMOS reset transistor M7 will be shorted and make both outputs equal: V_{out}+ = V_{out}− while NMOS transistor M8 is off. During evaluation phase (Clk=V_{dd}), as the reset transistor M7 is off and the tail transistor of the latch M8 is on, the comparison will be made by a positive feedback formed from back-to-back cross coupled inverter pairs (M4/M6 and M5/M7). While this comparator shows faster speed and consumes less power, it generates more kickback noise and during reset phase both outputs (V_{out}+, V_{out}−) are not reset exactly to either V_{dd} or 0V. It can be concluded that pre-amplifier based latched comparators, which is a combination of a pre-amplifier and a latch, offer fast speed and low offset while they still consume static power.

3. Proposed Comparator

3.1 Differential Current Sensing Comparator

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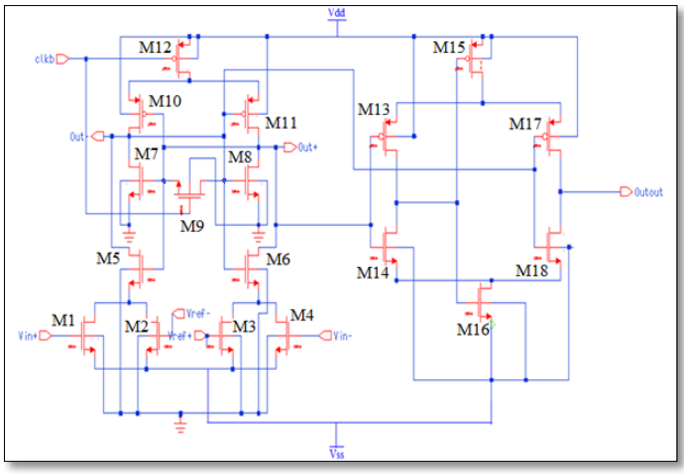

Figure 8. Schematic of Differential Current Sensing Comparator [2]

The Differential Current Sensing Comparator was introduced in [5]. Whenever the Clk signal goes low the circuit enters in regenerative mode. Transistor M12 is on and M7 is off. When values of both the outputs Out^+ and Out^- increases above threshold voltage of nMOS M5 and M6, both will start conducting which will connect the outputs with comparing circuit at the input side. It consumes more power because unless and until final state is reached both the outputs must drive common mode currents. The comparing circuit used at the input side consisting of transistors M1, M2, M3 and M4 are used to transfer the difference of the input voltage into differential currents. During reset interval, a pass transistor M7 is used to connect both the outputs together. The two outputs Out^+ and Out^- of differential current sensing comparator are being converted into single output with the output buffer circuit so that various analysis can be carried out.

3.2 Charge Sharing Dynamic Latch Comparator

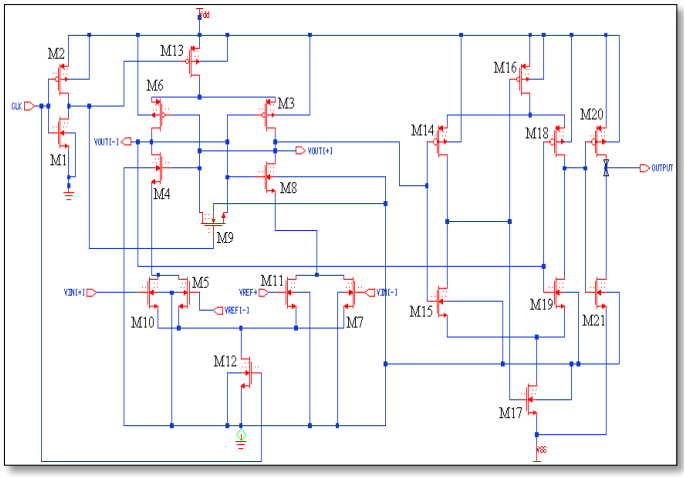

Figure 9. Schematic of Charge Sharing Dynamic Latch Comparator [3]

This topology combines the good features of the other two of dynamic latch comparator that suitable with pipeline A/D converters which is resistive dividing comparator and differential current sensing comparator [2]. The nMOS transistor M12 is used in series with resistive comparing circuit for regenerative mode in order to achieve low power. For reset mode pMOS pre charging circuit is absent and nMOS transistor M9 for output pass transistor for the equalization of both the voltages nearly to $V_{dd}/2$. Now, when the clock goes low, V_{dd} and ground both will be disconnected from the latch with the help of transistors M12 & M3. The two ended output of the dynamic charge sharing comparator are V_{out+} & V_{out-}. Both the outputs of the comparator are inputs to the buffer. Thus, the two ended output of dynamic charge sharing comparator is being converted into single ended output for different types of analysis.

3.3 Referred High Performance CMOS Voltage Comparator

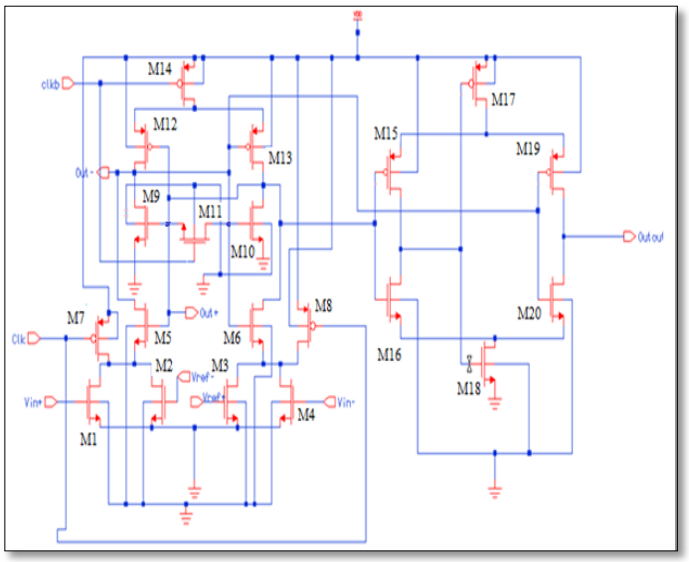

Figure 10. Schematic of Proposed High Speed CMOS Voltage Comparator

Whenever the Clk signal goes high, the circuit enters in regenerative mode. Transistor M11 and M7 are off and M14 is on. When values of both the outputs Out^+ and Out^- increases above threshold voltage of nMOS M5 and M6, both will start conducting which will connect the outputs with comparing circuit at the input side. The comparing circuit used at the input side consisting of transistors M1, M2, M3 and M4 are used to transfer the difference of the input voltage into differential currents. During reset interval, a pass transistor M11 is used to connect both the outputs together. Whenever the Clk signal goes low, transistor M7 and M8 are on. The two nodes which relate to the drains of M7 and M8 will get reset to V_{dd}. These internal nodes are reset to V_{dd} during the phase when the comparator is not deciding. This will ensure that all the internal nodes are reset before the comparator goes into decision mode. So, the problem associated with previous code dependent biased decision which occurs due to the charge imbalance left from previous decision at one of the nodes of the comparator which affects next decision is thus removed.

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The two outputs Out+ and Out- of the comparator are being converted into single output with the output buffer circuit so that various analysis can be carried out.

3.4 Modified High Performance CMOS Voltage Comparator

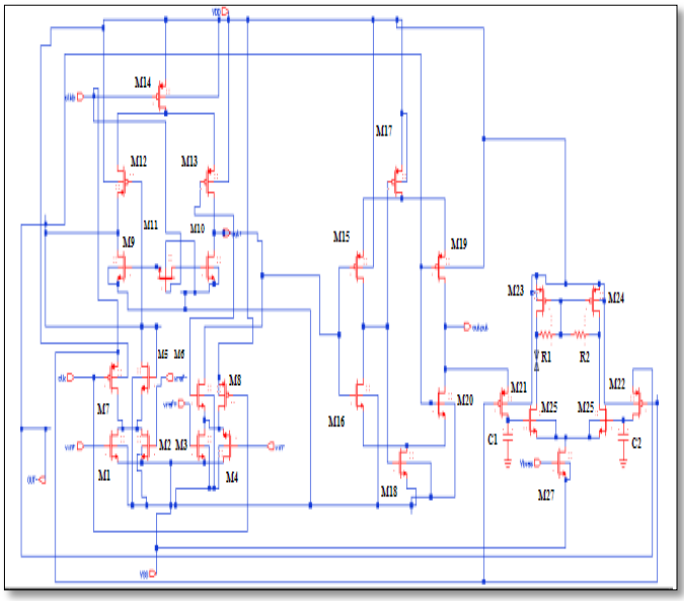

Figure 11. Modified High Performance CMOS Voltage Comparator

Whenever the Clk signal goes high, the circuit enters in regenerative mode. Transistor M11 and M7 are off and M14 is on. When values of both the outputs Out+ and Out- increases above threshold voltage of nMOS M5 and M6, both will start conducting which will connect the outputs with comparing circuit at the input side. The comparing circuit used at the input side consisting of transistors M1, M2, M3 and M4 are used to transfer the difference of the input voltage into differential currents. During reset interval, a pass transistor M11 is used to connect both the outputs together. Whenever the Clk signal goes low, transistor M7 and M8 are on. The two nodes which relate to the drains of M7 and M8 will get reset to Vdd. These internal nodes are reset to Vdd during the phase when the comparator is not deciding. This will ensure that all the internal nodes are reset before the comparator goes into decision mode. So, the problem associated with previous code dependent biased decision which occurs due to the charge imbalance left from previous decision at one of the nodes of the comparator which affects next decision is thus removed. The two outputs Out+ and Out- of the comparator are being converted into single output with the output buffer circuit so that various analyses can be carried out. In the offset cancellation phase, Clkb becomes high and Clk becomes low which causes transistor 21 and 22 on bringing the offset cancellation block into action. The offset cancellation feedback-loop consists of a differential pair with active load. Its common mode voltage is set by resistive common mode feedback R1 and R2. When Clkb moves to logic low with Clk at logic low state, offset cancellation phase stops.

4. Simulation Result

4.1 Simulation Results of Differential Current Sensing Comparator

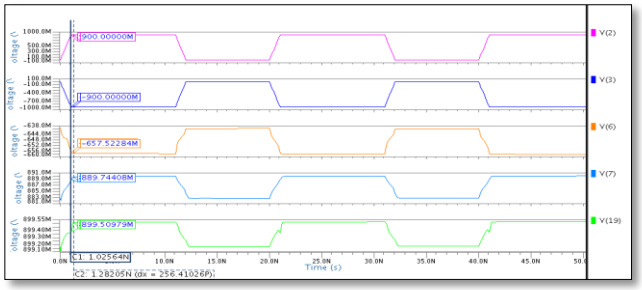

Figure 12. Transient Response of Differential Current Sensing Comparator in TSMC 90nm Technology

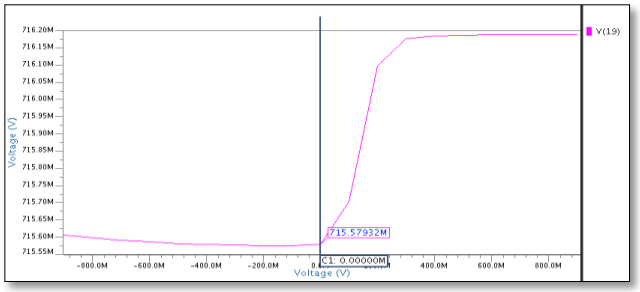

Figure 13. Offset Voltage of Differential Current Sensing Comparator in TSMC 90nm Technology

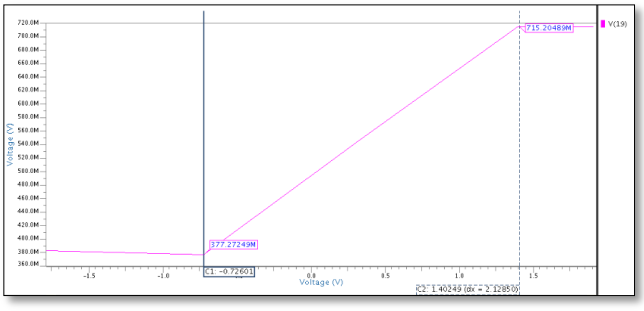

Figure 14. Input Common Mode Range of Differential Current Sensing Comparator in TSMC 90nm Technology

4.2 Simulation Results of Charge Sharing Dynamic Latch Comparator

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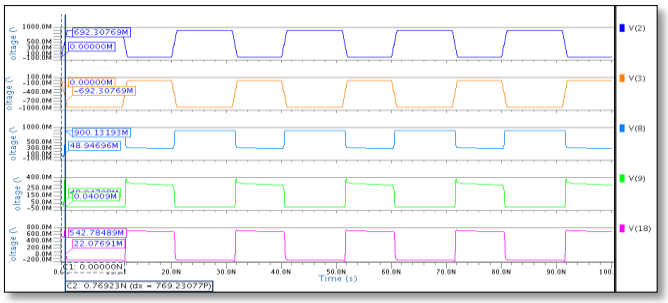

Figure 15. Transient Response of Charge Sharing Dynamic Latch Comparator in TSMC 90nm Technology

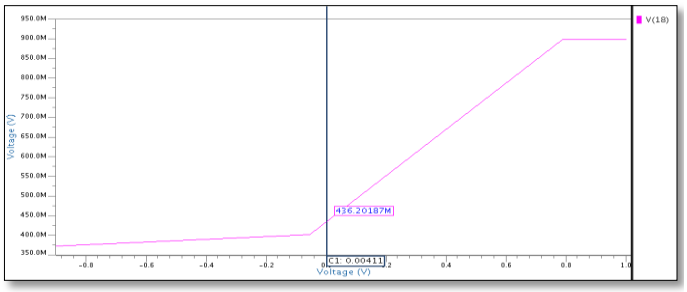

Figure 16. Offset Voltage of Charge Sharing Dynamic Latch Comparator in TSMC 90nm Technology

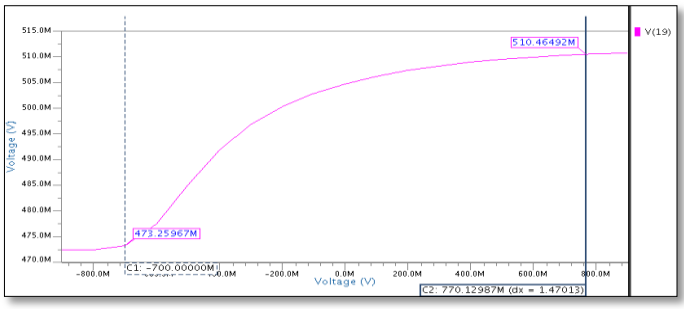

Figure 17. Input Common Mode Range of Charge Sharing Dynamic Latch Comparator in TSMC 90nm Technology

4.3 Simulation Results of Referred High Performance CMOS Voltage Comparator

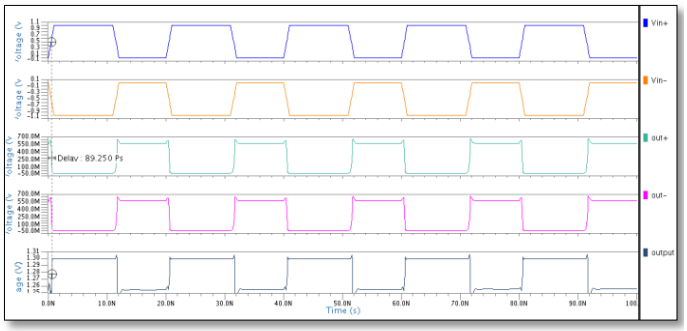

Figure 18. Transient Response of Referred High Performance CMOS Voltage Comparator in TSMC 90nm Technology

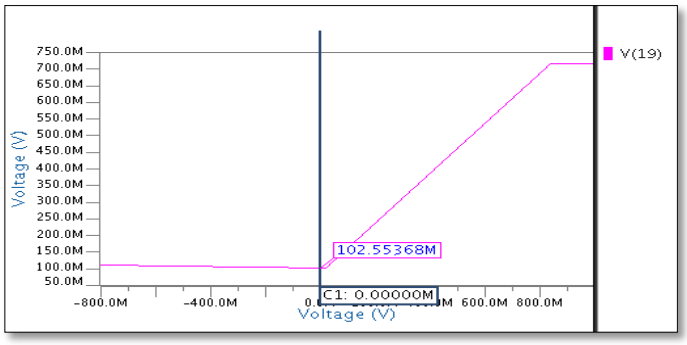

Figure 19. Offset Voltage of Referred High Performance CMOS Voltage Comparator in TSMC 90nm Technology

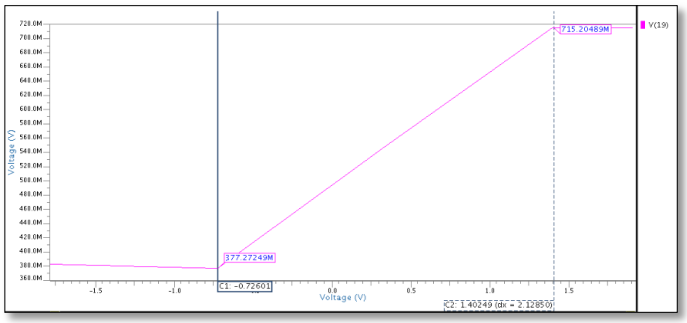

Figure 20. Input Common Mode Range of Referred High Performance CMOS Voltage Comparator in TSMC 90nm Technology

4.4 Simulation Results of Modified High Performance CMOS Voltage Comparator

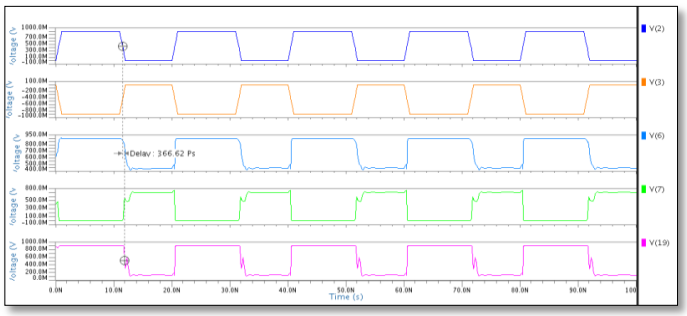

Figure 21. Transient Response of Modified High Performance CMOS Voltage Comparator in TSMC 90nm Technology

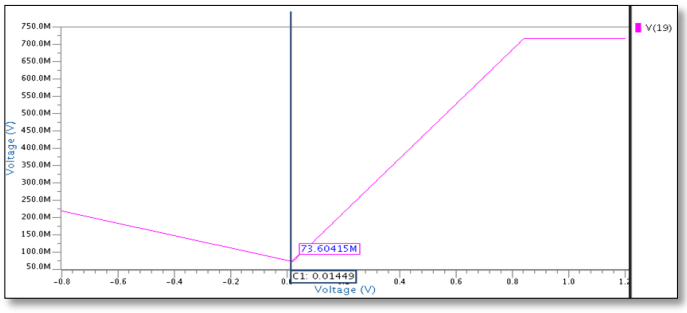

Figure 22. Offset Voltage of Modified High Performance CMOS Voltage Comparator in TSMC 90nm Technology

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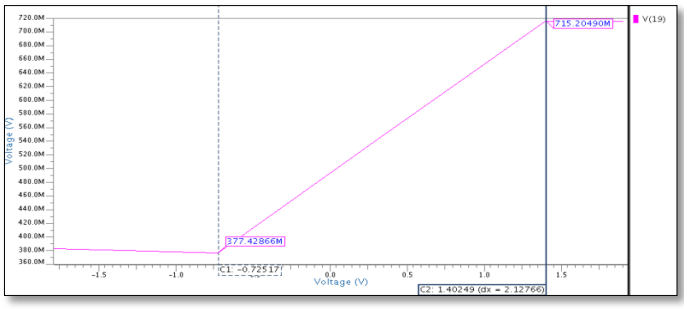

Figure 23. Input Common Mode Range of Modified High Performance CMOS Voltage Comparator in TSMC 90nm Technology

5. Conclusion

In this paper, various type of comparators suitable for low power high speed applications have been characterized and simulated. The comparator is designed in TSMC Generic 90nm technologies. The comparator is characterized in terms of the offset, propagation delay, ICMR, power dissipation. The simulation results allow the circuit designer to fully explore the tradeoffs in comparator design, such as delay, offset voltage, and power Dissipation for Analog to Digital Converters. In the modified design offset reduction block was introduced in the comparator topology of Dynamic Latch Comparator. This modified architecture showed low offset voltage and high speed as compared to other architectures of the comparator.

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Table 1. Comparative Analysis of Different Architectures of Voltage Comparator in 90nm Technology

Parameters	**Differential Current Sensing Comparator**	**Charge Sharing Dynamic Latch Comparator**	**Referred High Speed CMOS Voltage Comparator**	**Modified CMOS Voltage Comparator**
Power Dissipation	11.7mW	4.77mW	6.12µW	5.8µW
Propagation Delay (ns)	0.256	0.769	0.089	0.366
Offset (V)	0.71	0.5	0.102V	0.073
ICMR (V)	-0.7 to 1.4	1 to 2	-0.1 to 0.8	-0.7 to 1.4