THINK INDIA (Quarterly Journal)

ISSN:0971-1260
Vol-22-Issue-4-October-December-2019

Closed Loop Control of Two Switch Buck Boost Converter with Low Voltage Stress

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Abstract-This paper presentsthe comparison of single switch and conventional continuous buck boost converter over proposed two switch buck boost converter for reduction of voltage stress across semiconductor devices and improvement of efficiency. In single switch converter voltage stress is high which is sum of input voltage and output voltage. Even though conventional TSBB converter reduces voltage stress, but increases the conducting losses. The proposed TSBB converterwhich have similar number of both active and passive components to conventional TSBB converter, decreases voltage stress and also there is decrease in conducting components losses .So efficiency of proposed TSBB converter is increased. The open loop proposed TSBB converter is made into closed loop control converter using PID controller of 48 V constant output voltages.Theproposed closed loop converter using PID controller enhances the dynamic stability performance of buck boost DC-DC converter. So that vigorous output voltage obtained against variations in the circuit components and changes in load disturbances.

Keywords:Two switch buck boost Converter (TSBB), reduced voltage stress,single switch buck boost converter (SSBB), low conducting losses, PID controller.

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Vol-22-Issue-4-October-December-2019

1. INTRODUCTION:

ISSN:0971-1260
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Many electric and electronic applications use DC –DC converters. Due to global warming issues which increases energy consumption. Now a day's energy consumption efficiency is important factor. The various converter applications are battery powered systems, fuel cells,self-regulating power supplies, power factor correction application. High efficiency is very important in many applications,to achieve these mainly DC - DC converter are used [1]-[3]. Duty ratio of the switch is necessary for steps up and step down modes of buck boost converter determination.If converter operates in buck modei.e. duty ratio is a smaller than 0.5 in steps down mode,and the converter which operates in boost mode i.e. duty ratio is greater than the 0.5 in buck mode.However converter have only one switch, one inductor and one diode in SSBB converter configuration .Figure1 single switch buck boost converter(SSBB). Therefore there is high voltage stress across semiconductor of SSBB which is sum of V_{in} and V_o. To cause voltage stress across semiconductor switch to a low value.Design a conventional two switch buck boost converter (TSBB) as shown in fig 2.

Fig 1: Single switch buck boost converter (SSBB)circuit diagram

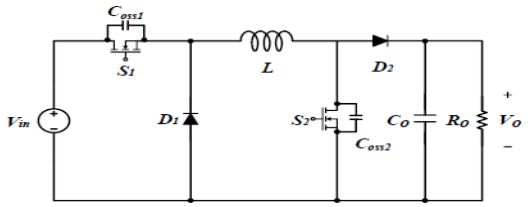
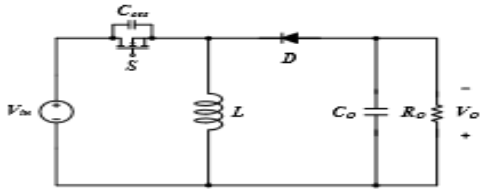


Fig 2 : Conventional two switch buck boost converter (TSBB)

The cascade connection of buck converter and the boost converter TSBB converter is obtained. It consists of one inductor,two switches, two diodes. Voltage stress across switch S_1,diode D_1 is V_{in} and across switch S_2,diode D_2 is V_o. The TSBB converter operate in buck mode, boost mode, and buck boost mode operating the switches S_1 and S_2.The TSBB converter operate in the step down mode ,when S_2 is in the off state and S_1 is to be controlled to get constant output voltage. When TSBB converter operated in the boost mode by keeping S_1 in on state and switch S_2 is to be controlled to get constant output voltage. When switches S_1 and S_2 are switched on and off at the same time, so the converter operates in buck boost mode. When this converter operate in buck boost



mode conducting components are increased compare to SSBB converter, that additional components when the switches are in on state L, S_1, S_2, are conducting components, and when switches are in off state L , D_1, D_2 , are conducting components. Thus additional components in every subinterval are one switch and one diode. Hencein conventional two switch buck boost converter (TSBB),overall switching losses and conducting losses are increased when it operates in buck boost mode. However, overall power losses in buck mode and in boost mode are reduced[4]-[5].

Theaverage inductor current and the root mean square same i.e.ripple of the inductor current in two switch buck boost converter is neglected. Average inductor current is $I_o/(1-d_2)$,where output current is I_o and the duty ratio of the switch S_2 is d_2.The average inductor current in buck mode is equal to output current $I_o$because d_2=0 i.e. switch S_2 is all time in off state. The average inductor current in boost mode and buck boost mode are different based on duty ratio d_2 of switch S_2. The average inductor current in boost mode is less than that of the buck boost mode. As a result conducting losses and switching losses in buck or boost mode a r e

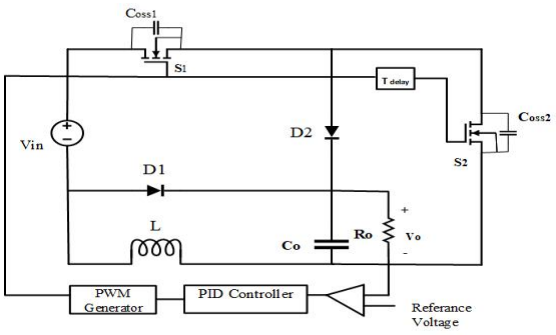


Fig 3: Closed loop control of proposed two switch buck boost converter circuit diagram.

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The problems of the SSBBand conventional TSBB converter were overcome by designing a new configuration of DC-DC buck boost converter which is shown in fig 3.The proposed converter andconventional TSBB converterhaving same number of components as [6]. By controlling the switches independently proposed converter operates in step down voltage mode, step up voltage mode, and buck boost mode also. Therefore proposed converter reduces voltage stresses and improves efficiency of the converter.

Here in this paper the quality of output is feedback to the pulse width modulator of active switches. PID controller is employed for the output voltage regulation by controlling pulse width of the active switches of a converter to the reference values making as a closed loop control.

2.BUCK BOOST CONVERTER OPERATION:

For getting of constant voltage of DC output, which is more than or smaller than the input voltage preferable to use buck Boost converter [7].
The converter which is proposed when operated in the continuous mode ofconduction, the output voltage

ISSN:0971-1260
Vol-22-Issue-4-October-December-2019

lesser when compare to buck boost mode of conventional two switch buck boost converter.Therefore the TSBB converter will get maximum efficiency in buck or boost operating mode even though it has difficulty of switch control compare to SSBB converter.

(1)

where the duty ratio of switches $S_1$and S_2 were $d_1$and d_2 respectively.

TABLE 1
Various converter components voltage stress comparison

Converter	Components			
	S_1	D_1	S_2	D_2
Proposed	V_{in}	$V_{in}+V_o$	V_o	V_o
TSBB	V_{in}	V_{in}	V_o	V_o
SSBB	$V_{in}+V_o$	$V_{in}+V_o$	N/A	N/A

The converter which is proposed and conventional converter Voltage stress were compared is as shown in Table1

TABLE 2
Conducting components comparison

Modes of operation	Subinterval	Proposed converter	TSBB converter
Buck mode	interval 1	S_1, D_2	S_1,D_2
	interval2	D_1	D_1,D_2
Boost mode	interval1	S_1,S_2	S_1,S_2
	interval2	S_1,D_2	S_1,D_2
Buck Boost mode	interval1	S_1,S_2	S_1,S_2
	interval2	D_1	D_1,D_2

Conducting components during switching operation in various subintervals were compared is shown in table 2

3. PROPOSED CONVERTER DESIGN AND ANALYSIS:

Proposed converter in closed loop circuit is shown in fig3 which have intrinsic output capacitors are C_{oss1} andC_{oss2} across the switches S_1 and S_2 respectively. Switch S_1 was controlled to get output voltage by keeping d_2=0, so proposed converter is operated in step down voltage mode.Similarly switch S_2 is controlled and switch S_1 is always in on state to get output voltage by keeping d_1=1, so the proposed converter operates in step up mode. Hence the operation of converter in buck boost mode switches were simultaneously turns on and turn off. This is explained based on equation(1). The conducting path of proposed converter in different modes of operation with subintervals shownin table 2.

3.1 Relation between voltage ratio and switches output capacitance:

The value of intrinsic output capacitance i.e.C_{oss1} and C_{oss2} across the two switches S_1 and S_2 are given based on given equation (2)

(2)

To attain likely voltage stresses across switches S_1 and S_2,so that turn-off delay is applied among switches to satisfy the equation (2). That effects the selection of switches.

3.2 Relation between Voltage ratio and Turn-Off Ratio:

During subinterval 1($t_0 \le t \le t_1$) S1 and S_2switches wereall together turned on at that interval. And in subinterval2 ($t_1 \le t \le t_2$) S_1 is still in on state and S_2 in off state. So that voltage across switch S_2 is held to V_0 by D_2.Lastly during subinterval 3 ($t_2 \le t \le t_3$) D_1 is in on state and S_1 is turned off. So that voltage across switch S_1 is V_{in}. Now turn off ratio can be written as

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(3)

The C_{oss2} was charged till voltage becomes V_o at T_{delay} duration and V_{Coss2} be written as

V_{Coss2}= (4)

Here $I_{L(turn\ off)}$shows inductor current after S_2 is off.

Hence turn off delay ratio $D_{off\ ratio}$ written as

(5)

Where supply frequency f_s=100kHz,$C_{oss2,equ}$ shows C_{oss2}average capacitance value, V_{in}=48.By substituting all other parameters $D_{off\text{-}delay}$ is equal to 0.01 to 5 fold margin. And that turn off delay is shown in figure 4.

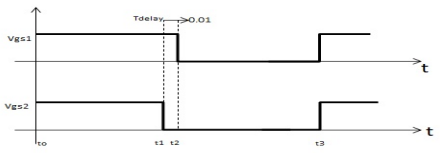

Fig 4 Turn off delay waveform between S_1 and S_2.

TABLE 3

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DESIGNED PARAMETER IN VARIOUS CONVERTER CONFIGURATION

Components		SSBB converter	TSBB converter	Proposed converter
Diode	D_1	MBR10H150 (V_F=0.87,V_{RRM}=150)	MBR10100 (V_F=0.8,V_{RRM}=100)	MBR10H150 (V_F=0.87,V_{RRM}=150)
	D_2	N/A	MBR1060 (V_F=0.8, V_{RRM}=60)	
Switch	S_1	FQ45N14V2 (Drain to source voltage=150v, Drain source On resistance=40mΩ)	FDPF085N10A (Drain to source voltage=100v, Drain source On resistance=39mΩ)	
	S_2	N/A	FQPF65N06 (Drain to source voltage=60v, Drain source On resistance=16mΩ)	
Inductor	L	160μH		

The conducting components losses in proposed converter during steps down mode and also in buck boost mode are less compared with TSBB converter. Butconducting components are same in boost mode in both TSBB and proposed converter. Overall conducting losses are fewer in proposed converter related with the two switch buck boost converter. Therefore efficiency is improved in closed loop proposed converter [8], [9].

4. BUCK BOOST CONVERTER IN CLOSED LOOP CIRCUIT USING PID CONTROLLER:

Open loop circuit is converted into closed loop circuit by comparing required output voltage with reference voltage value. By this the switching pulses are controlled automatically. Discrete PID controller is one of the preferable controllers which enhance dynamic stability and transient stability without affecting the stable state error of that proposed converter.And its block diagram had shown in figure5.

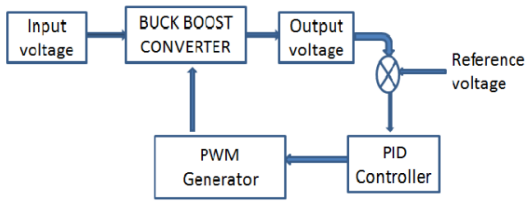

Fig 5 : Buck Boost Converter block diagram with PID Controller.

The samples that are obtained from output voltage passes through the pulse width modulator generate gating pulses for controlling of switches automatically [10], [11].There is time delay of 0.01sec between both switch S_1 and switch S_2 which is shown in fig 4. Based on the condition in equation (2), intrinsic output capacitor values are selected.

5. SIMULATION RESULTS:

By using Matlab/Simulink software by components parameters shown in Table 3.The Closed loop proposed converter was designed by input voltage of V_{in}=72v,switching frequency f_s=100 kHz, with constant output voltage V_o=48v, and P_o=150w. Here two switches are used with a capacitor across it with a value of 666.66 μF and 1000μF for C_{oss1} ,C_{oss2} respectively. The turn off delay timeis 0.01 sec of proposed converter in buck boost mode to get voltage on S_2 equal to 48v.

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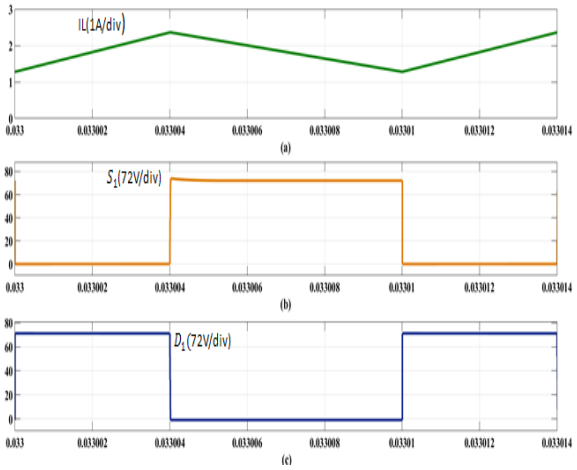

Fig 6: Proposed converter Simulink waveform without closed loop in step down mode for V_{in}=72v

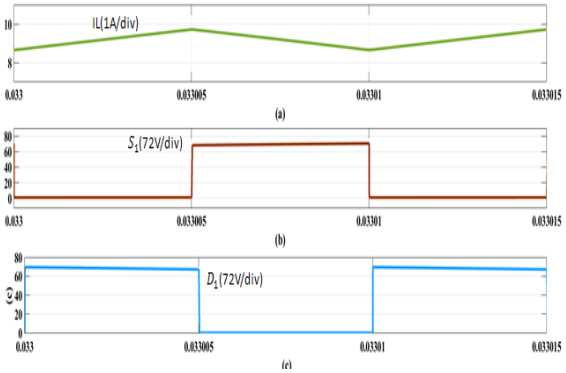

Fig 7: Proposed converter Simulink waveforms without closed loop in step up mode for V_{in}=36

When output power is 150w proposed converter measured efficiency is 89.3% in buck boost mode. Hence in proposed converter switches controlled independently to get maximum efficiency with controlling switches independently as shown in fig 8.

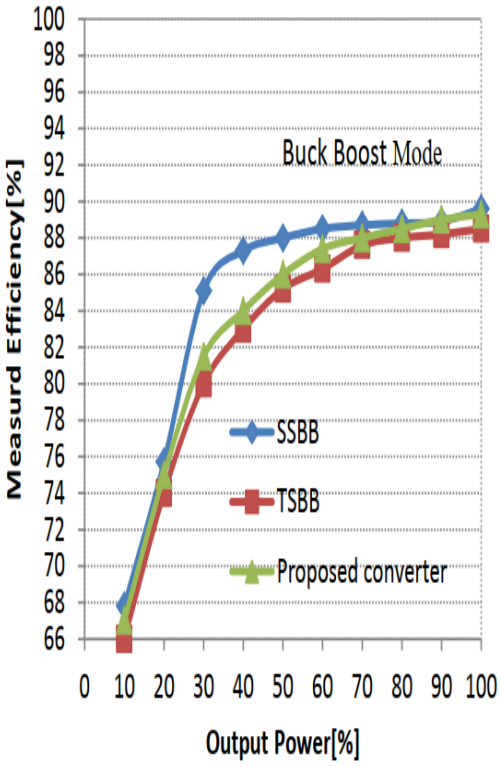

Fig 8: Measured Efficiency at V_{in}=72v, V_o=48V, f_S=100 KHz and output power P_o=15-150w

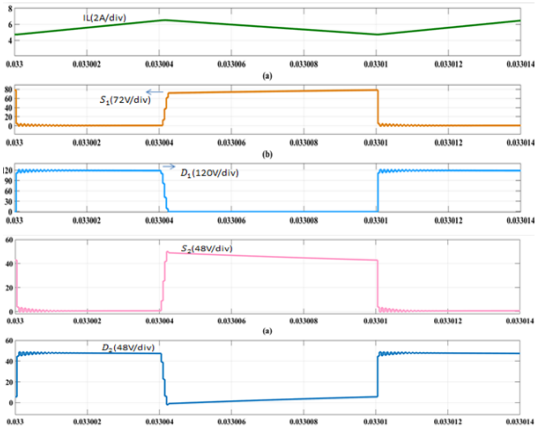

Fig 9: Proposed converter Simulink results without closed loop in buck boost converter for V_{in}=72v

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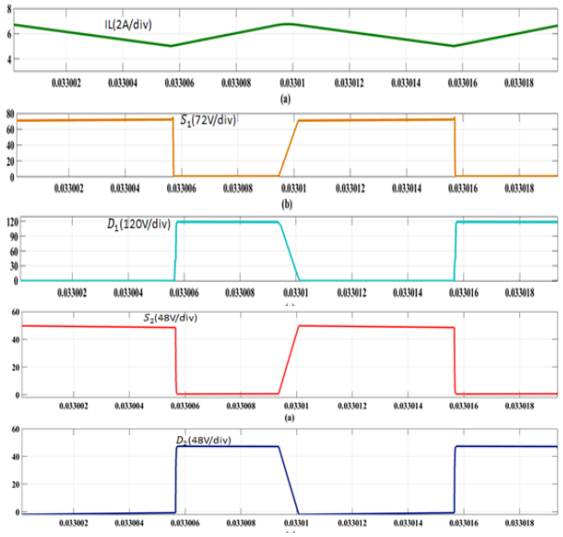

Fig 10 : Simulation results of closed loop control of proposed converter for V_{in}=72v in buck boost converter

Proposed converter without closed loop operating in step down mode, steps up mode simulation results shown in fig 6 and fig 7 respectively. Voltage across S_1 and D_1 is equal to 72V. Buck Boost mode simulation results of proposed converter as shown in fig 9. Voltage stress on both S_2 and D_2 is V_o=48 as shown in fig 9 and fig 10.

Closed loop converter is designed using PID controller and is tuned by P=0.066, I=0.45 and D=0, simulation results shown in fig 10.The tuning of PID controller is by trial and error method.

6. CONCLUSION:

This paper presents a new closed loop DC-DC Buck Boost Converter was proposed. Compare to SSBB converter,proposed converter voltage stresses across any semi-conductor device is reduced. And in proposed converter conducting component losses are reduced compare with TSBB converter. In practical application there is a possibility of changes in load and circuit parameters, which causes changes in circuit operation. To defeat this type of problem, designing of suitable controller is required. For this PID controller is more preferable to attain constant output voltage of 48v from 72v input voltage. So that switching pulses were regulated automatically using PID controller and also there is increase in dynamic stability of proposed converter.

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ISSN:0971-1260
Vol-22-Issue-4-October-December-2019